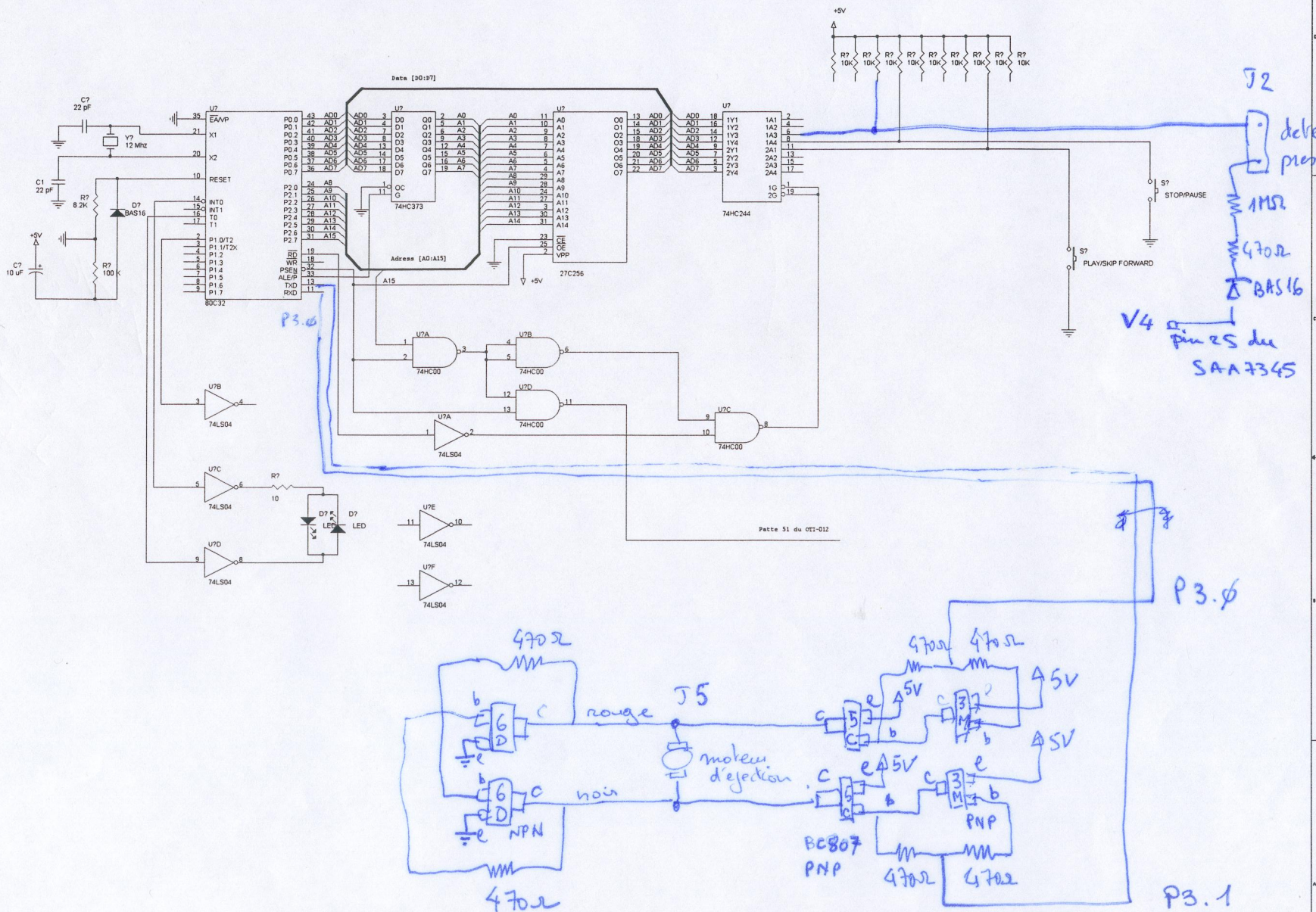
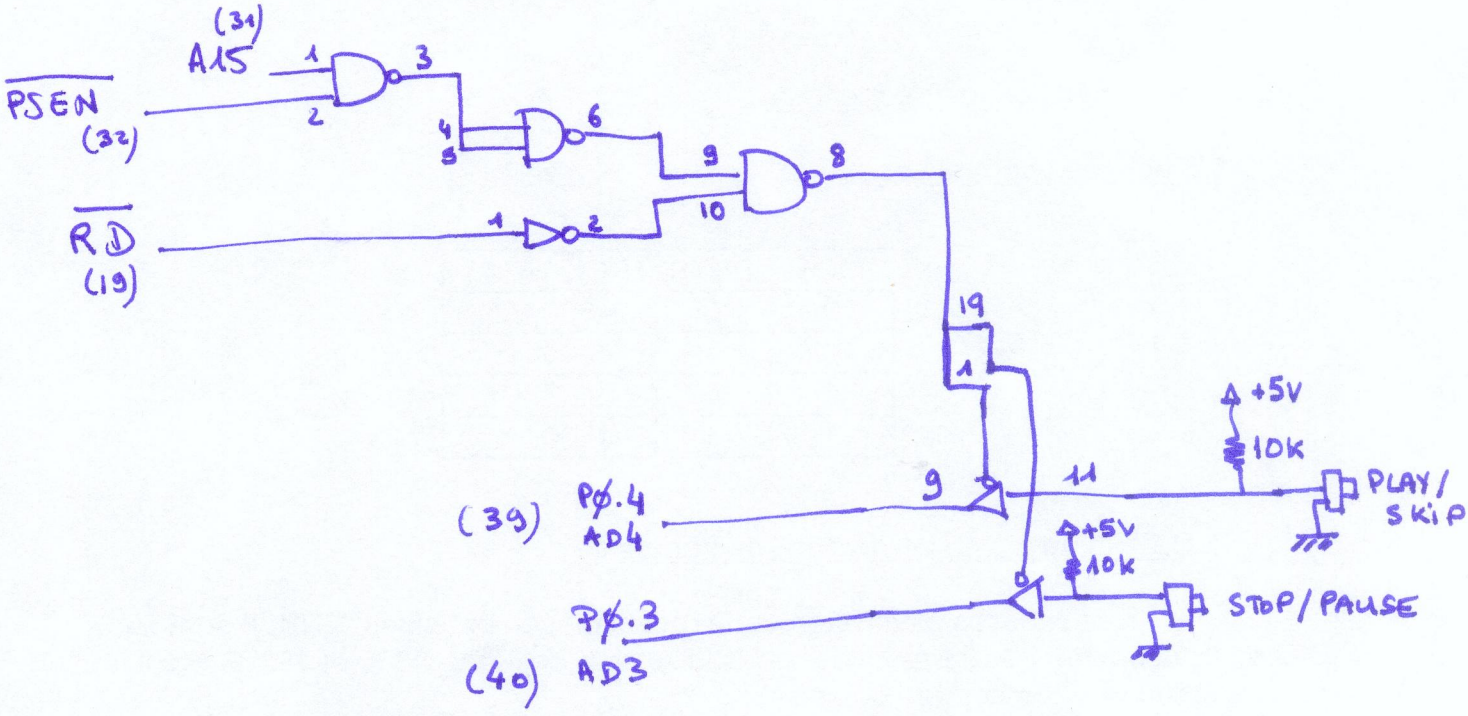
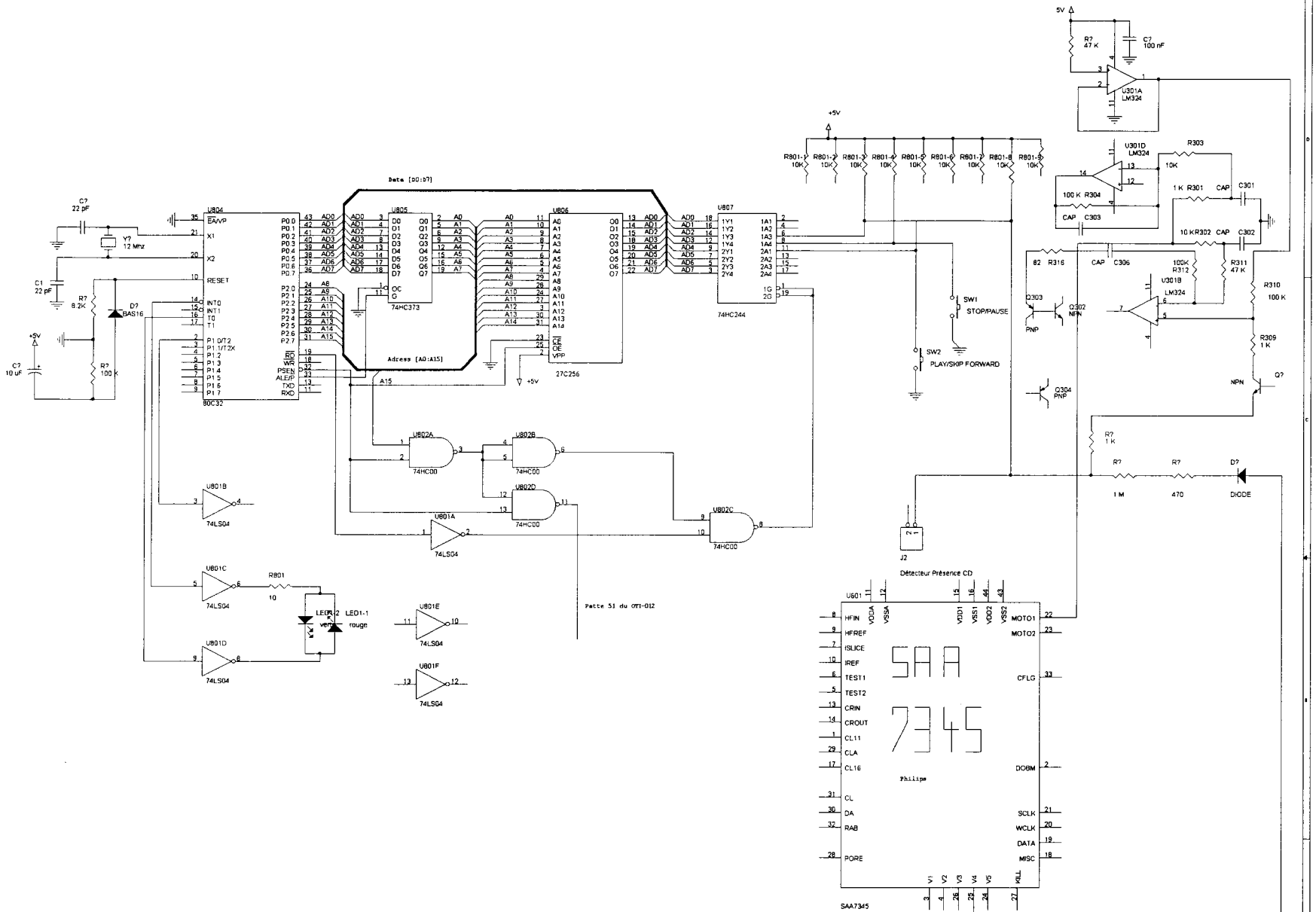

Data [D0:D7]
Adress [A0:A15]
80C32
74HC373
74HC244
27C256
74HC00
74LS04
BAS16
LED
12 Mhz
22 pF
8.2K
100
10 uF
10
+5V
R? 10K
S? STOP/PAUSE
S? PLAY/SKIP FORWARD
J2
détecteur présence CD.
1MΩ
470Ω
V4
pin 25 du SAA7345
P3.0
P3.1
P3.0
J5
rouge
noir
moteur d'éjection
NPN
PNP
BC807 PNP
5V
Patte 51 du OTI-012
J
Wearnes CDD110 CDROM Drive Schematics
Document Number (Doc)
Monday, September 13, 1999



$\overline{PSEN}$ selectionne la memoire programme externe

$\overline{RD}$ selectionne la mémoire donnée externe



Title	Wearnes CDD110 CDROM Drive Schematics	
Size C	Document Number (Doc)	Rev 0.0
Date: Monday, September 13, 1999	Sheet 1 of 1	

3A83 → setb P3.1
setb P3.Ø
ret

3A88 setb P3.1
clr P3.Ø

3A8D setb P3.Ø
clr P3.1
ret

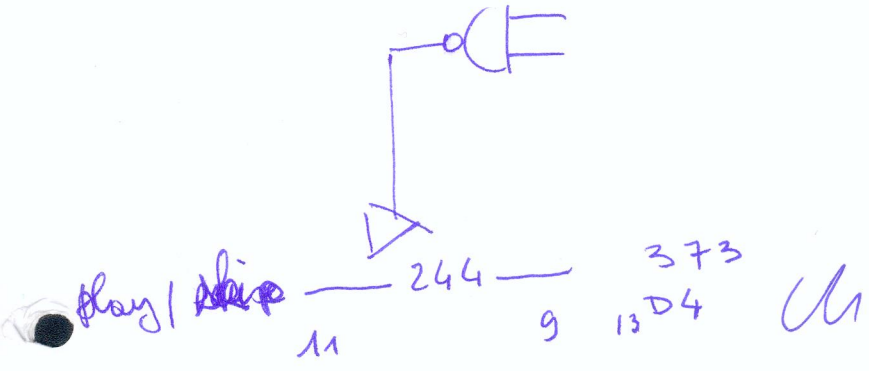
□

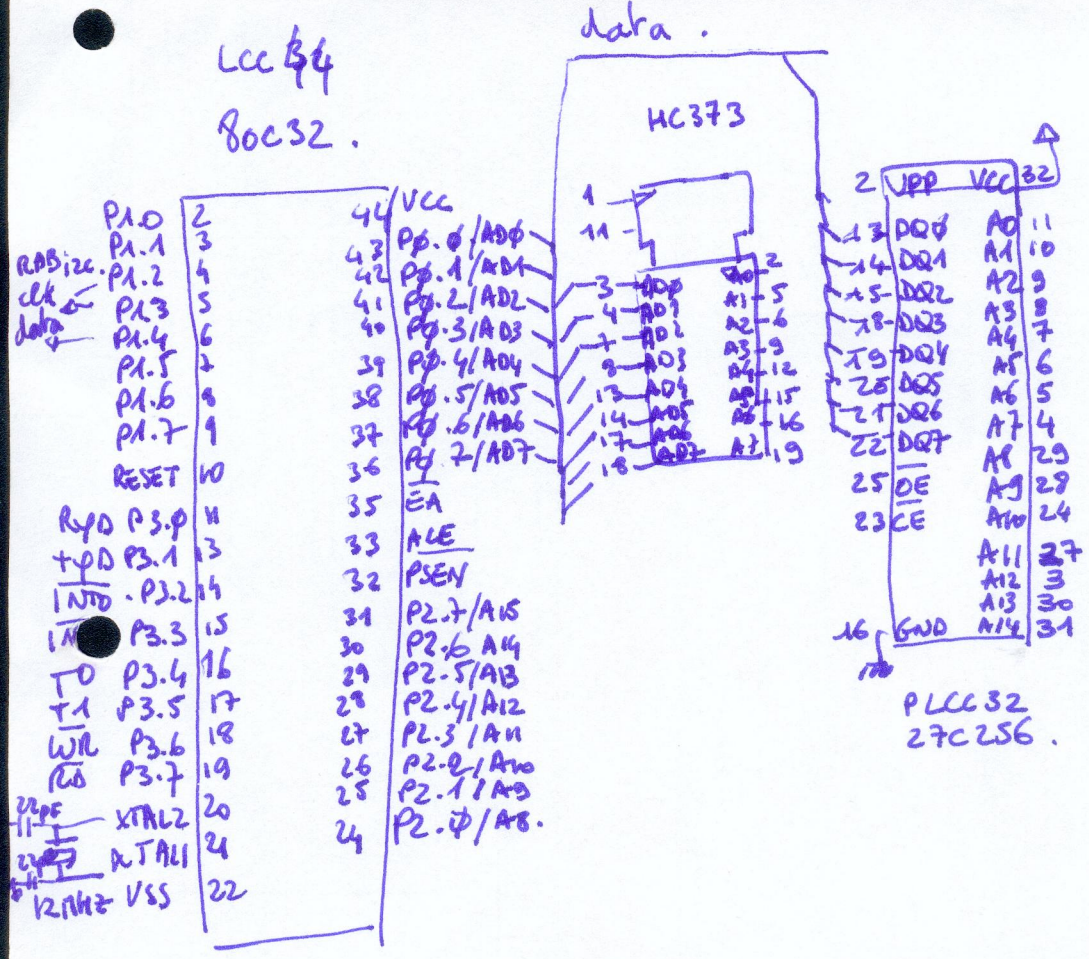
3A9F
3ABØ
4540 4600 4684 47FE
45AC 461F 46CØ 473B

ejectum CD

l3F7B.

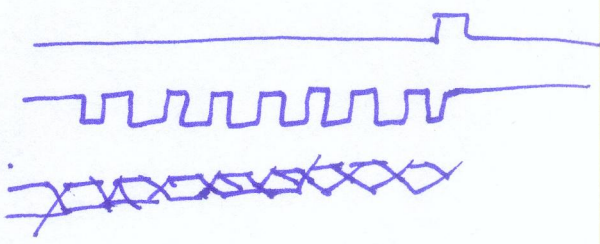
ch 37H.
mov 08h, #01Fh.
lcall l3951
mov 00B, #00Eh.
lcall. C3951





0000 0
0001 1
0010 2
0011 3
0100 4
0101 5
0110 6
0111 7
1000 8
1001 9
1010 10. A
1011 11 B
1100 12 C
1101 13 D
1110 14 E
1111 15 F

18H. play
ou 1Fh.



ecriture I2C

l3991.

```
mov   A, 008H.DA.
setb  data.
clr   rab
mov   rp, #008H.
clr   clk.
rlc   A.
mov   data, C
nop.
setb  clk
djnz  R0, L3999
Setb  rab.
```

mémoire
08H = buffer i2c

l3999

C6, 14, 30, 28, B3, DE, 6B
AA, 42, 50,

envoi
20H. BBH.
42H. 18H.
44H. 1DH.
40H. C6H.
42H. 30H.
1EH. 62H
1CH. 00H
1BH. 01H
B3H. C2H.
DBH.
1FH
DEH.
1AH.

```
L6391   lcall L8C83                          ; play?
        JNC  L6385
        mov  008, #1F                       ; motor mode play mode.
        lcall  ℓ3991
        mov  008 #00EH                      ; V5 = 1.
        lcall  ℓ3991
        mov  a, #00H
        ret.

ℓ6385   mov  A, 01BH.
        jnz     ℓ63C8.
        jnb  035H, ℓ63C5
        mov  1BH, #07DH
        clr  035H.
        clr  A
        ret.
```

STANDARD MODE PIN-OUT ASSIGNMENT

Standard Mode Pin-Out Assignment if pin 28 is tied to Vss.

Pin	Pin Name	Type	Comments	Pin	Pin Name	Type	Comments
1	Vss	P	Vss	41	Vss	P	Vss
2	RAD[6]	O	RA6	42	UD[3]	B	D3
3	RAD[7]	O	RA7	43	UD[4]	B	D4
4	RAD[8]	O	RA8	44	UD[5]	B	D5
5	RAD[9]	O	RA9	45	UD[6]	B	D6
6	RAD[10]	O	RA10	46	UD[7]	B	D7
7	RAD[11]	O	RA11	47	URS	I	RS
8	RAD[12]	O	RA12	48	URDB	I	/RD
9	RAD[13]	O	RA13	49	UWRB	I	/WR
10	RAD[14]	O	RA14	50	UCSB	I	/CS
11	RAD[15]	O	RA15	51	UINTB	O	/INT
12	RWEB	O	/RWE	52	Vss	P	Vss
13	Vss	P	Vss	53	RESETB	I	/RESET
14	ROEB	O	/ROE	54	HCSB	I	/ENABLE
15	N/C	-	Unused	55	HWRB	I	/HWR
16	RD[7]	B	IO8	56	HRDB	I	/HRD
17	RD[6]	B	IO7	57	HCMDB	I	/CMD
18	RD[5]	B	IO6	58	HWAITB	O	/WAIT
19	RD[4]	B	IO5	59	HDTENB	O	/DTEN
20	RD[3]	B	IO4	60	HSTENB	O	/STEN
21	RD[2]	B	IO3	61	HEOPB	O	/EOP
22	RD[1]	B	IO2	62	RCSB	O	/RCS
23	RD[0]	B	IO1	63	-	O	Unused
24	Vss	P	Vss	64	Vss	P	Vss
25	XIN	I	EXTAL	65	HD[7]	B	HD7
26	XOUT	O	XTAL	66	HD[6]	B	HD6
27	TEST1	I	TESTA	67	HD[5]	B	HD5
28	ENHANCE	I	0:Standard 1:Enhanced	68	HD[4]	B	HD4
29	DCSEL	I	CSEL	69	HD[3]	B	HD3
30	DLMSEL	I	LMSL	70	HD[2]	B	HD2
31	Vdd	P	Vdd	71	HD[1]	B	HD1
32	DLRCK	I	LRCK	72	HD[0]	B	HD0
33	DSDATA	I	SDATA	73	Vdd	P	Vdd
34	DBCK	I	BCK	74	HSELDRQB	I	/SELDRQ
35	N/C	-	Unused	75	RAD[0]	O	RA0
36	DC2PO	I	C2PO	76	RAD[1]	O	RA1
37	MCK	O	MCK	77	RAD[2]	O	RA2
38	UD[0]	B	D0	78	RAD[3]	O	RA3
39	UD[1]	B	D1	79	RAD[4]	O	RA4
40	UD[2]	B	D2	80	RAD[5]	O	RA5

ENHANCED MODE PIN-OUT ASSIGNMENT

Enhanced Mode Pin-Out Assignment if pin 28 is tied to Vdd.

	Pin Name	Type	Comments		Pin Name	Type	Comments
	Vss	P	Vss		Vss	P	Vss
	RAD[6]	O	RA6		UD[3]	B	D3
	RAD[7]	O	RA7		UD[4]	B	D4
	RAD[8]	O	RA8		UD[5]	B	D5
	RAD[9]	O	RA9		UD[6]	B	D6
	RAD[10]	O	RA10		UD[7]	B	D7
	RAD[11]	O	RA11		URS	I	RS
	RAD[12]	O	RA12		URDB	I	/RD
	RAD[13]	O	RA13		UWRB	I	/WR
	RAD[14]	O	RA14		UCSB	I	/CS
	RAD[15]	O	RA15		UNITB	O	/INT
	RWEB	O	/RWE		Vss	P	Vss
	Vss	P	Vss		RESETB	I	/RESET
	ROEB	O	/ROE		HCSB	I	/ENABLE
	HA1	I	Host Address 1		HWRB	I	/HWR
	RD[7]	B	IO8		HRDB	I	/HRD
	RD[6]	B	IO7		HA0	I	Host Address 0
	RD[5]	B	IO6		HDRQ	O	Host Data Request
	RD[4]	B	IO5		HDRQEB	O	Host DRQ Enable
	RD[3]	B	IO4		HFBLB	O	Host First Byte Latch
	RD[2]	B	IO3		HFBC	O	Host First Byte Cycle
	RD[1]	B	IO2		RCSB	O	/RCS
	RD[0]	B	IO1		HRSTB	O	Reset from Host
	Vss	P	Vss		Vss	P	Vss
	XIN	I	EXTAL		HD[7]	B	HD7
	XOUT	O	XTAL		HD[6]	B	HD6
	EJECT	I	Disk Door Eject switch		HD[5]	B	HD5
	ENHANCE	I	0:Standard 1:Enhanced		HD[4]	B	HD4
	DCSEL	I	CSEL		HD[3]	B	HD3
	DLMSEL	I	LMSL		HD[2]	B	HD2
	Vdd	P	Vdd		HD[1]	B	HD1
	DLRCK	I	LRCK		HD[0]	B	HD0
	DSDATA	I	SDATA		Vdd	P	Vdd
	DBCK	I	BCK		HSELDRQB	I	/SELDRQ
	HDACKB	I	Host Data Acknowledge from DMA controller		RAD[0]	O	RA0
	DC2PO	I	C2PO		RAD[1]	O	RA1
	MCK	O	MCK		RAD[2]	O	RA2
	UD[0]	B	D0		RAD[3]	O	RA3
	UD[1]	B	D1		RAD[4]	O	RA4
	UD[2]	B	D2		RAD[5]	O	RA5

CR563 Panasonic. Carte LMJB0187A

NM27C256N - 120.

3130 CR-5620.80W. → fichier CR562.bin.

µC [M] MN 188 2410 V9E / 446A 3910
japan.

SANYO LC 98000. / A 910 4 JBUG

[M] MN 662710 RA / 4464 SI 25

National AN 8803 NSB

Sharp LH5P864 V-80.

[M] 8388 SR. 74HC00.

4N05. LS244. LS00
LS245 LS05

6285 FS / 4B26.

5216485 sur carte LMJB0187B

CD-ROM. GCD-R420 Goldstar

Samsung KS9241 / 340. @ 33,8 MHz.
Samsung KS9211B / 414B + TDA 1311A (DAC)
Motorola MPC1715FB
Goldstar GSH6433276 / 643327825F @ 20MHz
Sony CXA1082BQ.
JRC 2100 4021G
JRC 3415 4054D.
JRC 4560 4045B
Sony CXA1081Q.

Switch
VR. TEØ TEI FEØ FEI

Switch.

TOFF SEAR TEST GND
