



VANTIS

BEYOND PERFORMANCE

Product Menu

An AMD Company

MACH® 4A Family

	V _{CC} (V)	Macrocells (PLD Gates)	Output Enables	Registers	I/O (V) Compatibility	Static I _{CC} (mA)	Commercial Speed Grade							Package											
								-5	-55	-6	-65	-7*	-10*	-12*	I/Os + (Dedicated Inputs)										
							t _{PD} (ns)	5	5.5	6	6.5	7.5	10	12	44-pin PLCC	44-pin TQFP	48-pin TQFP	100-pin PQFP	100-pin TQFP	144-pin TQFP	176-pin TQFP	208-pin PQFP	256-ball BGA	352-ball BGA	
							t _{SS} (ns)	3	3.5	4	4	5.5	6	7											
							t _{COS} (ns)	4	4	4.5	4.5	5	5.5	6.5											
f _{CNT} (MHz)	182	167	154	154	125	118	95																		
M4A5-32/32 M4A3-32/32	5 3.3	32 (1250)	32	32	5/3.3	TBD		X					X	X	X	32 (2)	32 (2)	32 (2)							
M4A5-64/32 M4A3-64/32	5 3.3	64 (2500)	32	96	5/3.3	TBD		X	X	X	X	X	X	X	X	32 (2)	32 (2)	32 (2)							
M4A5-96/48 M4A3-96/48	5 3.3	96 (3750)	48	144	5/3.3	TBD		X	X	X	X	X	X	X	X				48 (8)						
M4A5-128/64 M4A3-128/64	5 3.3	128 (5000)	64	192	5/3.3	TBD		X					X	X	X			64 (6)	64 (6)						
M4A5-192/96 M4A3-192/96	5 3.3	192 (7500)	96	288	5/3.3	TBD		X	X	X	X	X	X	X	X					96 (16)					
M4A5-256/128 M4A3-256/128	5 3.3	256 (10000)	128	384	5/3.3	TBD		X	X	X	X	X	X	X	X								128 (14)	128 (14)	
M4A3-384	3.3	384 (15000)	192	576	5/3.3	TBD																132	160	192	
M4A3-512	3.3	512 (20000)	256	768	5/3.3	TBD																132	160	192	256

Advance Information

All MACH 4A devices have SpeedLocked™ performance at ≤ 20 product terms per output.
All MACH 4A devices have JTAG-ISP capability.

MACH 4 Family

	V _{CC} (V)	Macrocells (PLD Gates)	Output Enables	Registers	I/O (V) Compatibility	Static I _{CC} (mA)	Commercial Speed Grade					Package													
								-7	-10*	-12*	-15*	I/Os + (Dedicated Inputs)													
							t _{PD} (ns)	7.5	10	12	15	44-pin PLCC	44-pin TQFP	48-pin TQFP	84-pin PLCC	100-pin PQFP	100-pin TQFP	144-pin TQFP	208-pin PQFP	256-ball BGA					
							t _{SS} (ns)	5.5	6	7	10														
							t _{COS} (ns)	5.5	6.5	8	10														
f _{CNT} (MHz)	111	95	77	56																					
M4-32/32 M4LV-32/32	5 3.3	32 (1250)	32	32	5/3.3	18		X	X	X	X	32 (2)	32 (2)	32 (2)											
M4-64/32 M4LV-64/32	5 3.3	64 (2500)	32	96	5/3.3	25		X	X	X	X	32 (2)	32 (2)	32 (2)											
M4-96/48 M4LV-96/48	5 3.3	96 (3750)	48	144	5/3.3	30		X	X	X	X							48 (8)							
M4-128/64 M4LV-128/64	5 3.3	128 (5000)	64	192	5/3.3	50		X	X	X	X				64 (6)	64 (6)									
M4-128N/64 M4LV-128N/64	5 3.3	128 (5000)	64	192	5/3.3	50		X	X	X	X			64 (6)											
M4-192/96 M4LV-192/96	5 3.3	192 (7500)	96	288	5/3.3	75		X	X	X	X								96 (16)						
M4-256/128 M4LV-256/128	5 3.3	256 (10000)	128	384	5/3.3	100		X	X	X	X											128 (14)	128 (14)		

* Industrial grades are available.

All MACH 4 devices have SpeedLocked™ performance at ≤ 20 product terms per output.
All MACH 4 devices, apart from the M4LV-128N/64, have JTAG-ISP capability.

MACH 5A Family

	V _{CC} (V)	Macrocells (PLD Gates)	Output Enables	I/O (V) Compatibility	Static I _{CC} (mA)	Commercial Speed Grade					Package							
											I/Os							
							-5	-6	-7*	-10*	-12*	100-pin TQFP	100-pin PQFP	144-pin TQFP	160-pin PQFP	208-pin PQFP	256-ball BGA	352-ball BGA
						t _{PD} (ns)	5.5	6.5	7.5	10	12							
						t _{SS} (ns)	3	3	4	5	6							
t _{COS} (ns)	4.5	5	6	7	8													
f _{CNT} (MHz)	182	167	125	100	83.3													
M5A5-128 M5A3-128	5 3.3	128 (5000)	16	5/3.3	TBD		X		X	X	X	74	68	104	120			
M5A5-192 M5A3-192	5 3.3	192 (7500)	24	5/3.3	TBD		X		X	X	X	74	68	104	120			
M5A5-256 M5A3-256	5 3.3	256 (10000)	32	5/3.3	TBD		X		X	X	X	74	68	104	120	160		
M5A3-320	3.3	320 (12500)	40	5/3.3	TBD		X	X	X	X	X				120	160	192	
M5A3-384	3.3	384 (15000)	48	5/3.3	TBD		X	X	X	X	X				120	160	192	
M5A3-512	3.3	512 (20000)	64	5/3.3	TBD		X	X	X	X	X				120	160	192	256

Advance Information

All MACH 5A devices have 4 Dedicated Inputs and up to 32 product terms per output.
All MACH 5A devices have JTAG-ISP capability.

MACH 5 Family

	V _{CC} (V)	Macrocells (PLD Gates)	Output Enables	I/O (V) Compatibility	Static I _{CC} (mA)	Commercial Speed Grade					Package									
											I/Os									
							-5	-7*	-10*	-12*	-15*	100-pin TQFP	100-pin PQFP	144-pin TQFP	144-pin PQFP	160-pin PQFP	208-pin PQFP	240-pin PQFP	256-ball BGA	352-ball BGA
						t _{PD} (ns)	5.5	7.5	10	12	15									
						t _{SS} (ns)	3	4	5	6	8									
t _{COS} (ns)	4.5	6	7	8	10															
f _{CNT} (MHz)	182	125	100	83.3	62.5															
M5-128 M5LV-128	5 3.3	128 (5000)	16	5/3.3	35 20		X	X	X	X	X	68 68, 74	68	104	104	120				
M5-192	5	192 (7500)	24	5/3.3	45			X	X	X	X	68	68		104	120	160			
M5-256 M5LV-256	5 3.3	256 (10000)	32	5/3.3	60 40		X	X	X	X	X	68 68, 74	68	104	104	120	160			
M5-320 M5LV-320	5 3.3	320 (12500)	40	5/3.3	55			X	X	X	X					120	160	184	192	
M5-384 M5LV-384	5 3.3	384 (15000)	48	5/3.3	60			X	X	X	X					120	160	184	192	
M5-512 M5LV-512	5 3.3	512 (20000)	64	5/3.3	80			X	X	X	X					120	160	184	192	256

* Industrial grades are available.

All MACH 5 devices have 4 Dedicated Inputs and up to 32 product terms per output.
All MACH 5 devices have JTAG-ISP capability.

Product Ordering Information

MACH 4, MACH 4A, MACH 5, and MACH 5A Families

Vantis programmable logic products are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

M4A3
-512
/256
-65
A
C

Family Type

M4A5 = MACH 4 Advanced Feature Set (5-V V_{CC}) M4 = MACH 4 Family (5-V V_{CC})
M4A3 = MACH 4 Advanced Feature Set (3.3-V V_{CC}) M4LV = MACH 4 Family Low Voltage (3.3-V V_{CC})
M5A5 = MACH 5 Advanced Feature Set (5-V V_{CC}) M5 = MACH 5 Family (5-V V_{CC})
M5A3 = MACH 5 Advanced Feature Set (3.3-V V_{CC}) M5LV = MACH 5 Family Low Voltage (3.3-V V_{CC})

Device Number

32 = 32 Macrocells 96 = 96 Macrocells 192 = 192 Macrocells 320 = 320 Macrocells
64 = 64 Macrocells 128 = 128 Macrocells 256 = 256 Macrocells 384 = 384 Macrocells
512 = 512 Macrocells

I/Os

/32 = 32 I/Os in 44-pin PLCC, 44-pin TQFP or 48-pin TQFP /120 = 120 I/Os in 160-pin PQFP
/48 = 48 I/Os in 100-pin TQFP /128 = 128 I/Os in 208-pin PQFP, 176-pin TQFP or 256-ball BGA
/64 = 64 I/Os in 84-pin PLCC, 100-pin PQFP or 100-pin TQFP
/68 = 68 I/Os in 100-pin PQFP or 100-pin TQFP /160 = 160 I/Os in 208-pin PQFP
/74 = 74 I/Os in 100-pin TQFP /184 = 184 I/Os in 240-pin PQFP
/96 = 96 I/Os in 144-pin TQFP /192 = 192 I/Os in 256-ball BGA
/104 = 104 I/Os in 144-pin PQFP or 144-pin TQFP /256 = 256 I/Os in 352-ball BGA

Operating Conditions

C = Commercial (0°C to +70°C)
I = Industrial (-40°C to +85°C)

Package Type

A = Ball Grid Array (BGA)
H = Plastic Quad Flat Pack with heat sink (PQFP)
J = Plastic Leaded Chip Carrier (PLCC)
V = Thin Quad Flat Pack (TQFP)
Y = Plastic Quad Flat Pack (PQFP)

Speed

-5 = 5 ns t_{PD} for MACH 4A -10 = 10 ns t_{PD}
or 5.5 ns for MACH 5(A) -12 = 12 ns t_{PD}
-55 = 5.5 ns t_{PD} -14 = 14 ns t_{PD}
-6 = 6 ns t_{PD} -15 = 15 ns t_{PD}
-65 = 6.5 ns t_{PD} -18 = 18 ns t_{PD}
-7 = 7.5 ns t_{PD} -20 = 20 ns t_{PD}

Valid Combinations

Refer to the menu pages or consult the local Vantis sales office to confirm the availability of specific valid combinations.

Device Marking

Actual device marking may differ from the ordering part number (OPN). "MACH 5" is marked on a device wherever "M5-" is used on the OPN.

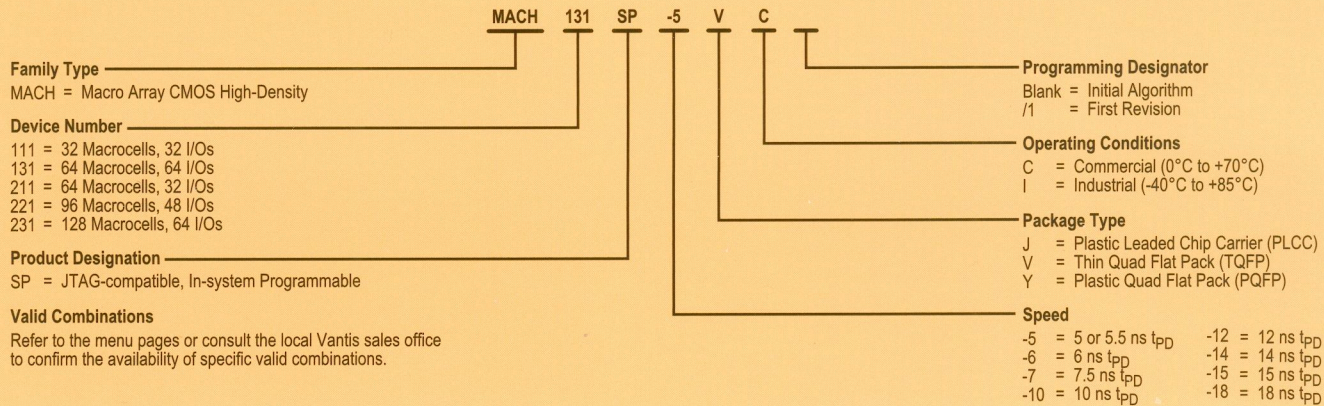
MACH 1 and 2 Families

	V _{CC} (V)	Macrocells (PLD Gates)	Output Enables	I/Os	Dedicated Inputs	JTAG-ISP	Static I _{CC} (mA)	Commercial Speed Grade						Package							
									-5	-6	-7	-10	-12	-15	44-pin PLCC	44-pin TQFP	68-pin PLCC	84-pin PLCC	100-pin PQFP	100-pin TQFP	
MACH111	5	32 (1250)	8	32	6	No	40	t _{PD} (ns)	5		7.5	10	12	15	X	X					
t _{SS} (ns)								3.5		5.5	6.5	7	10								
t _{COS} (ns)					3.5			5	6	8	10										
f _{CNT} (MHz)					182			133	100	76.9	66.6										
MACH111SP					2	Yes															
MACH131	5	64 (2500)	16	64	6	No	75	t _{PD} (ns)	5.5		7.5	10	12	15							
t _{SS} (ns)								3		5.5	6.5	7	10								
t _{COS} (ns)					4			5	6	8	10										
f _{CNT} (MHz)					182			133	100	76.9	66.6										
MACH131SP					6	Yes															
MACH211	5	64 (2500)	8	32	6	No	40	t _{PD} (ns)		6*	7.5	10	12	15	X	X					
t _{SS} (ns)									5*	5.5	6.5	7	10								
t _{COS} (ns)						4*		4.5	6	8	10										
f _{CNT} (MHz)						166*		133	100	83.3	66.6										
MACH211SP					2	Yes															
MACH221	5	96 (3750)	16	48	8	No	70	t _{PD} (ns)			7.5	10	12	15			X				
t _{SS} (ns)										5.5	6.5	7	10								
t _{COS} (ns)								5	6	8	10										
f _{CNT} (MHz)								133	100	83.3	66.6										
MACH221SP					8	Yes															
MACH231	5	128 (5000)	16	64	6	No	135	t _{PD} (ns)		6**	7.5**	10	12	15							
t _{SS} (ns)									5**	5.5**	6.5	7	10								
t _{COS} (ns)						4**		5**	6.5	8	10										
f _{CNT} (MHz)						166**		133**	100	83.3	66.6										
MACH231SP					6	Yes	80														

Parameters marked with a "*" are for the MACH211SP version only.
Parameters marked with a "**" are for the MACH231 non-SP version only.
MACH 1 devices have up to 12 product terms per output.
MACH 2 devices have up to 16 product terms per output.

Product Ordering Information

MACH 1 and 2 Families



CMOS PAL® Family

	I/Os	Dedicated Inputs	Max. PT per Output	Features	Speed Grade							Commercial	Industrial	20-pin PLCC	20-pin PDIP	20-pin SOIC	24-pin PDIP	24-pin SOIC	28-pin PLCC	28-pin PDIP		
					-5	-7	-10	-12	-15	-20	-25											
PALCE16V8H	8	10	8	Half Power	X							X		X								
						X						X		X	X	X						
PALCE16V8Q						Quarter Power			X				X	X	X	X	X ¹					
											X			X	X	X						
PALCE16V8Z						Zero Power				X				X	X	X						
												X	X	X	X	X	X					
PALLV16V8				3.3V			X				X	X	X	X								
PALLV16V8Z				3.3V, Zero Power						X		X	X	X								
PALCE20V8H	8	14	8	Half Power	X							X							X			
									X	X					X	X				X	X	
PALCE20V8Q				Quarter Power					X		X	X					X	X				
										X	X	X ²	X				X	X				
PALCE22V10H	10	12	16	Half Power	X							X							X			
									X						X	X				X	X	
									X					X	X				X	X		
										X				X	X				X	X		
											X			X	X				X	X		
												X		X	X				X	X		
PALCE22V10Q				Quarter Power			X		X		X	X				X	X					
PALCE22V10Z					Zero Power				X			X	X				X	X				
											X	X	X				X	X				
PALLV22V10				3.3V		X					X	X										
							X					X	X				X	X				
PALLV22V10Z				3.3V, Zero Power							X	X				X	X					
PALCE24V10H	10	16	8	Half Power				X		X	X						X	X				
PALCE26V12H	12	8	16	Half Power		X					X	X						X				
										X	X	X		X	X					X	X	
PALCE29M16H	16	5	16							X	X					X	X					
PALCE29MA16H	16	5	12	Asynchronous CLK						X	X					X	X					
PALCE610H	16	4	8	Asynchronous CLK				X		X	X					X	X					
PALCE20RA10H	10	10	4	Asynchronous CLK		X					X	X										
										X	X	X	X	X	X				X	X		

1. Commercial devices only.
2. Q-25 only.

Product Ordering Information

CMOS PAL Family

Vantis programmable logic products are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

PAL CE 16 V 8 H -5 J C /5

Family Type _____

PAL = Programmable Array Logic

Technology _____

CE = CMOS Electrically Erasable
LV = Low Voltage operation, 3.3-V JEDEC compatible,
CMOS Electrically Erasable

Number of Array Inputs _____

Output Type _____

M = Advanced Macrocell V = Versatile
MA = Advanced Asynchronous Macrocell RA = Registered Asynchronous

Number of Flip-Flops or Outputs _____

Power _____

H = Half Power Q = Quarter Power Z = Zero Power

Valid Combinations

Refer to the menu pages or consult the local Vantis sales office to confirm the availability of specific valid combinations.

Programming Designator

Blank = Initial Algorithm
/4 = First Revision
/5 = Second Revision (Same Algorithm as /4)

Operating Conditions

C = Commercial (0°C to +70°C)
I = Industrial (-40°C to +85°C)

Package Type

J = Plastic Leaded Chip Carrier (PLCC)
P = Plastic DIP (PDIP)
S = Plastic Gull-Wing Small Outline Package (SOIC)

Speed

-5 = 5 ns t_{PD} -12 = 12 ns t_{PD} -20 = 20 ns t_{PD}
-7 = 7.5 ns t_{PD} -15 = 15 ns t_{PD} -25 = 25 ns t_{PD}
-10 = 10 ns t_{PD}

Vantis Software Offerings

			PC Development Systems	Workstation Development Systems	Migration Products	Maintenance Products	
Software Product			DesignDirect Base DesignDirect Vista DesignDirect Summit Floating Node	DesignDirect Summit Floating Node	Summit Floating License Upgrade	Vista Maintenance Summit PC Floating Node Maintenance Summit WS Floating Node Maintenance	
Part Number			DD-VISTA-PC-N DD-SUMMIT-PC-F	DD-SUMMIT-WS-F	MP-SUMMIT-PC-F	MA-VISTA-PC-N MA-SUMMIT-PC-F MA-SUMMIT-WS-F	
Features	Device Support	MACH 4 and MACH 4A	X X X	X			
		MACH 5 and MACH 5A	X X X	X			
		MACH 2	X X X	X			
		MACH 1	X X X	X			
		PAL	X X X	X			
	Design Entry	VHDL	X X				
		Verilog	X X				
		Schematic	X X X				
		ABEL	X X X	X			
	Simulation	VHDL RTL	X X				
		Verilog RTL	X X				
		Timing	X X				
		Functional	X X X	X			
	CAE Netlists	EDIF 2 0 0 Input	X X X	X			
		Verilog Output	X X X	X			
		VHDL Output	X X X	X			
		SDF Output	X X X	X			
		EDIF Output	X X X	X			
	CAE Libraries	Viewlogic	X X X	X			
		Synopsys Design Compiler	X X X	X			
		Synopsys FPGA Compiler	X X X	X			
		Mentor Design Architect	X X X	X			
		Cadence Concept	X X X	X			
	Productivity Tools	Performance Analyst	X X X	X			
		Constraints Editor	X X X	X			
	O/S	Windows '95/98/NT	X X X				
		Sun Solaris		X			
		HP-Unix		X			
	License	Single User	X X				
		Floating Node		X	X	X	
	Maintenance Product			N/A MA-VISTA-PC-N MA-SUMMIT-PC-F	MA-SUMMIT-WS-F	MA-SUMMIT-PC-F	

Notes:
 Download DesignDirect™ Base from www.vantis.com or order literature PID # DD-BASE-1.0 to obtain CD-ROM.
 Schematic capture not available on workstations.

Trademarks

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Please consult your local Vantis sales channel to verify availability or lead time of any device shown in this menu.



BEYOND PERFORMANCE

995 Stewart Drive, P.O. Box 3755,
 Sunnyvale, CA 94088

(408) 616-8000 • Toll Free: 1-888-VANTIS2
 www.vantis.com

Technical Support & Literature Ordering

Technical Support, USA, Toll Free: 1(888)826-8471

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FAR EAST: Fax (852)2956-2502

UK & EUROPE: +44-(0)1276-803285, Fax: +44-(0)1276-803298

FRANCE: 0800-908621 • GERMANY: 089-450-53199 • ITALY: 1678-77224

Europe Technical Support E-mail: euro.tech@vantis.com

Europe Literature Request E-mail: euro.lit@vantis.com