Programmable Peripherals Design and Applications Handbook

1992

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General Information

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Company Profile

Company Description

WSI is a market leading producer of high-performance programmable peripheral integrated circuits. The company was founded in 1983 to serve the needs of system designers who need to achieve higher system performance, reduce the size and power consumption of their systems, and shorten their product development cycles in order to achieve faster market entry.

WSI produces an innovative portfolio of Programmable Peripherals as well as a broad line of high-performance non-volatile programmable PROM and EPROM memory products, both based on its patented self-aligned split-gate CMOS EPROM technology. The new Programmable Peripherals enable rapid system design of high-performance application specific controllers and related products. These devices are the first to integrate high-performance EPROM, SRAM and user-configurable logic and deliver a performance and integration breakthrough to the programmable peripherals market.

WSI's Programmable Peripherals and non-volatile memory products enable electronic designers to reduce their system size, shorten product development cycles and bring new system products to market in less time. As a result, WSI has established itself as a leading supplier of high-performance programmable solutions to a broad customer base that includes some of the world's largest and most technologically advanced electronics companies.

Technology

WSI's patented self-aligned, split-gate EPROM technology enables higher performance and greater memory densities per chip area than the traditional stacked-gate method. By developing significantly higher read current, the WSI EPROM cell has enabled the development of several memory devices that are the fastest of their type on the market. This core NVM technology is further leveraged by WSI's architecture and design innovations such as staggered virtual ground and contactless memory arrays resulting in dramatic die area savings. This high density memory capability enables WSI to provide cost-effective market leading products such as the smallest 4-Mbit EPROM on the market. WSI's proprietary NVM technology (licensed to Sharp Corporation and National Semiconductor Corporation) has enabled WSI to be first in the industry with numerous product breakthroughs in speed, high density, process innovations and packaging.

Markets and Applications

WSI's Programmable Peripheral and high-performance non-volatile memory products are used by the world's leading suppliers of advanced electronic systems in telecommunications, data processing, military, automotive and industrial markets.

Applications for the Programmable Peripherals include cellular telephones, disk drive controllers, modems, bus controllers, engine management computers, telecom switchers, motor controllers and others. High performance memory applications include digital signal processing, engineering workstations, high-speed modems, video graphics controllers, radar and others. By virtue of their high speed and programming capability, WSI products are ideally suited for these applications where designers are pushing the limits of system performance in highly competitive markets.

Product Groups

Programmable Peripherals

WSI's family of Programmable Peripherals represents a new class of programmable products. They enable system designers to reduce the size of their products, achieve lower operating power, optimize system performance and shorten product development cycles. They are the first devices to integrate high-speed EPROM, SRAM and programmable logic on a single chip. The Programmable Peripherals include the PSD3XX family, the MAP168 and the PAC1000.

PSD3XX Family: Microcontroller Peripherals with Memory

Each member of the PSD3XX family is a single-chip, field-programmable circuit that integrates all the required peripheral memory and logic elements for an embedded-control design. Programmable logic, page logic, programmable I/O ports, busses, address mapping, port address/data tracking, 256K to 1 Mb EPROM, and 16K SRAM are all on board. Advanced features such as memory paging, microcontroller port reconstruction, track mode, configuration security bit, and cascading further enhance the utility and value of the PSD3XX family. PSD3XX family devices are ideal for applications requiring high-performance, low power and very small form factors such as fixed disk control, cellular telephones, modems, computer peripherals, and automotive and military applications.

MAP168 User-Configurable Peripheral with Memory

Similar to the PSD3XX family, the high speed MAP168 integrates high-performance EPROM, SRAM, a PAD and user-configurable logic. Ideal for high-speed applications requiring expanded memory, system integration and increased data security, the 45 ns MAP168 is used with high speed digital signal processors, microprocessors and microcontrollers.

PAC1000 Peripheral Controller

The high speed PAC1000 sets a new standard for Programmable Peripheral performance, integration and functionality. The PAC1000 replaces up to 50 complex devices in high-end embedded controllers and microprocessor-based systems. Combining a CPU, 1K x 64 EPROM and extensive user-configurable logic, the PAC1000 assists its host processor with high rates of data manipulation and control, freeing the processor for other system functions. The 16 MHz PAC1000 has been designed into numerous high-performance applications such as work-station direct memory access controllers, video imaging digital signal processors, and VME bus LAN controllers.

Programmable Peripheral Development Tools

WSI's Programmable Peripheral products are supported with complete easy-to-use system development tools from both Data I/O and WSI. The Data I/O Unisite programmer can be used for production programming. The WSI tools include program development, simulation, and programming software, the IBM-PC hosted MagicPro™ Memory and Peripheral Programmer, a dial-in applications bulletin board and WSI's team of factory service and field application engineers. The menu-driven software tools run on popular customer owned computers and enable designers to rapidly configure and program the WSI part and try it in a prototype system. Additional design iterations are quickly accomodated. The system development tools increase the efficiency of the design process resulting in faster market entry for WSI's customers' products.

High-Performance Memory Products

WSI offers a broad product line of high-performance CMOS PROMs and EPROMs featuring architectures ranging from 2K x 8 to 512K x 8, plus several x16 products, with speeds ranging from 25 to 150 ns. Commercial, industrial and military products including MIL-STD-883C/SMD are available. A wide variety of package selections include plastic and hermetic, through-hole and surface mount types.

CMOS PROMs

As WSI's fastest family of products, Re-Programmable Read Only Memories (RPROMs) provide high-speed bipolar PROM pinout with matching speed and low power operation. The product family includes architectures ranging from 2K x 8 to 32K x 8 with speeds ranging from 25 to 90 ns. Commercial, industrial and military MIL-STD-883C/SMD configurations are available in a variety of hermetic and plastic package types.

"F" Family EPROMs

The high-speed "F" series EPROM family offers speeds ranging from 35 to 70 ns and architectures from 8K x 8 to 32K x 8, plus several x16 products. "F" family EPROMs are ideal for use in high-end engineering and scientific workstations, data communications and similar high-performance applications.

"L" Family Military EPROMs

WSI's "L" family military EPROM memory products feature high-density and high speed in popular JEDEC pinouts. With speeds ranging from 120 to 300 ns and architectures from 64K x 8 to 512K x 8 including several x16 products, the "L" family offers significant speed and high density benefits for developers of military avionics, communications, and control systems. The "L" family delivers world class densities from WSI's conservative 1.2 micron lithography CMOS process technology.

Manufacturing

WSI's manufacturing strategy includes utilizing multiple world-class manufacturing partners for each facet of the production process.

WSI has licensed its CMOS EPROM and logic process technology to Sharp Corporation in Japan and National Semiconductor Corporation in the USA. The Sharp facility in Fukuyama, Japan employs the most advanced sub-micron VLSI integrated circuit manufacturing equipment available including ion implantation, reactive ion etch, and wafer stepper lithographic systems. The world-class high volume National Semiconductor operation delivers low cost production of 1.2 micron CMOS technology product on 6" wafers. This low defect density manufacturing resource is capable of producing sub-micron technology product in the near future.

High-volume, low cost integrated circuit packaging and testing is performed for WSI by ANAM Electronics in Seoul, Korea, Fine Products in Hsinchu,Taiwan, National Semiconductor in Santa Clara, CA and at WSI in Fremont, CA. ANAM is the largest independent manufacturer of I.C. packaging and produces excellent product quality. Test capability ranges from simple logic devices to complex VLSI product. ANAM routinely processes a wide variety of high volume packages and enables WSI to leverage its materiel needs through ANAM's combined high-volume, low cost procurement activity. Commercial, industrial, and military grade product processing is available from ANAM.

Additional quality assurance and reliability testing are performed at WSI in Fremont, CA.

WSI's manufacturing strategy ensures the supply of double-sourced high quality, high-volume product with low variable cost and fast delivery.

Sales Network

WSI's international sales network includes several regional sales managers who direct the resources of the company to major market opportunities. Experienced technical field application engineers located in each field office assist WSI's customers during their advanced product development and match customer needs with WSI's product solutions. Over sixty manufacturer's representatives and leading national and regional component distributors in the United States, Europe and Asia round out the WSI sales network.

United States

Direct sales and field application engineering offices in Boston, Chicago, Huntsville, Philadelphia, Dallas, Los Angeles and Fremont, CA; More than 25 manufacturer's representatives for major national accounts; national distributors include Arrow/Schweber, Time Electronics and Wyle Laboratories; and regional distributors.

International

Direct WSI Sales management offices in Paris, Munich and Hong Kong; sales representatives and distributors in Germany, England, France, Italy, Sweden, Finland, Denmark, Norway, Spain, Belgium, Luxembourg, the Netherlands, and Israel. Sales representatives and distributors for the Asia/Pacific Rim region in Japan, Korea, Taiwan, Hong Kong, Singapore and Australia.

Management and Previous Affiliations:

Michael Callahan
President, CEO and
Chairman of the Board
(Advanced Micro Devices, Monolithic Memories, Motorola)

Robert J. Barker
V. P. Finance, CFO and Secretary
(Monolithic Memories, Lockheed)

John Ekiss
V. P. Marketing
(Intel, Motorola)

Thomas Branch
V. P. Worldwide Sales
(Monolithic Memories, Fairchild)

George Kern
V. P. Operations
(Advanced Micro Devices, Monolithic Memories)

Boaz Eitan
V. P. New Product and Technology Development
(Intel)

Bob Buschini
Director of Human Resources
(General Electric, Raychem)

Financing

WSI is a privately held California corporation founded in August, 1983. The company has been financed by corporate investors, institutional investors, venture capital groups and private investors. Corporate investors are Sharp Corporation, National Semiconductor Corporation, Intergraph Corporation, and Kyocera Corporation. Venture capital investors include Accel Partners, Adler and Company, Bessemer Venture Partners, Genevest Consulting Group S. A., J. H. Whitney, Oak Investment Partners, Robertson Stephens and Co., Smith Barney Venture Corporation, and Warburg Pincus. The company has been audited annually since its inception by Ernst & Young (Arthur Young prior to 1989) and regularly reports financial information to Dunn & Bradstreet (Dunns number is 10-209-8167).

PROGRAMMABLE SYSTEM™ DEVICE FITS MULTIPLE MICROCONTROLLERS

IC HAS EPROM, RAM, AND LOGIC FOR 45 CONFIGURATIONS; INTERFACES 8- AND 16-BIT MICROCONTROLLERS.

MILT LEONARD

The embedded-controller market embraces a myriad of 8- and 16-bit microcontroller architectures that can satisfy just about any conceivable application requirement. However, each different controller requires its own unique combination of discrete devices to link the part to other system elements. Furthermore, changing application requirements usually call for restructuring I/O ports. Consequently, the application may eventually outgrow system memory and shared resources may demand multiple chip solutions. This means that in addition to comparing controllers on the merits of price and performance, prospective users must also consider the external circuitry that the controller needs to interface to the rest of the system.

A new chip from WaferScale Integration Inc., Fremont, Calif., simplifies system integration by combining RAM, EPROM, programmable decoding, and configurable I/O ports that expand 8- or 16-bit microcontrollers when they run out of on-chip resources. WaferScale's PSD301 is the first single-chip solution to offer a microcontroller with port expansion, latched address lines, a programmable address decoder (PAD), an expansion interface to shared resources, a 256-kbit EPROM, and a 16-kbit static RAM. In addition, the chip links directly to popular 8- and 16-bit microcontrollers without using glue logic.

The PSD301 architecture is a major enhancement of WaferScale's MAP168 mappable memory chip introduced last year *(see* ELECTRONIC DESIGN, *July 28, 1988, p. 91)*. In addition to the memory, decoding, and multiplexer functions of the 168, the 301 includes three software-configurable 8-bit I/O ports (A, B, and C), configuration registers, latched inputs, more chip-select lines, and more control on the strobe lines *(Fig. 1)*. Like the 168, a programmable security bit is given to protect against reverse engineering.

Most controllers can't be reprogrammed once they're configured. Moreover, their controller's I/O ports are designed to perform one of two mutually exclu-

USER-CONFIGURABLE MICROCONTROLLER INTERFACE

sive functions: convey control signals to peripheral devices or address and data signals to shared resources. Supplying both of these functions requires a multiple chip solution.

Microcontrollers also differ in boot-up locations and address mapping in memory. The 8051 and 8096 microcontrollers, for example, locate boot-up sequences in the lower half of their memory maps, while the 80186/88 and 68HCXXX use a high memory boot-up address. Another factor is the differences in control-signal polarities.

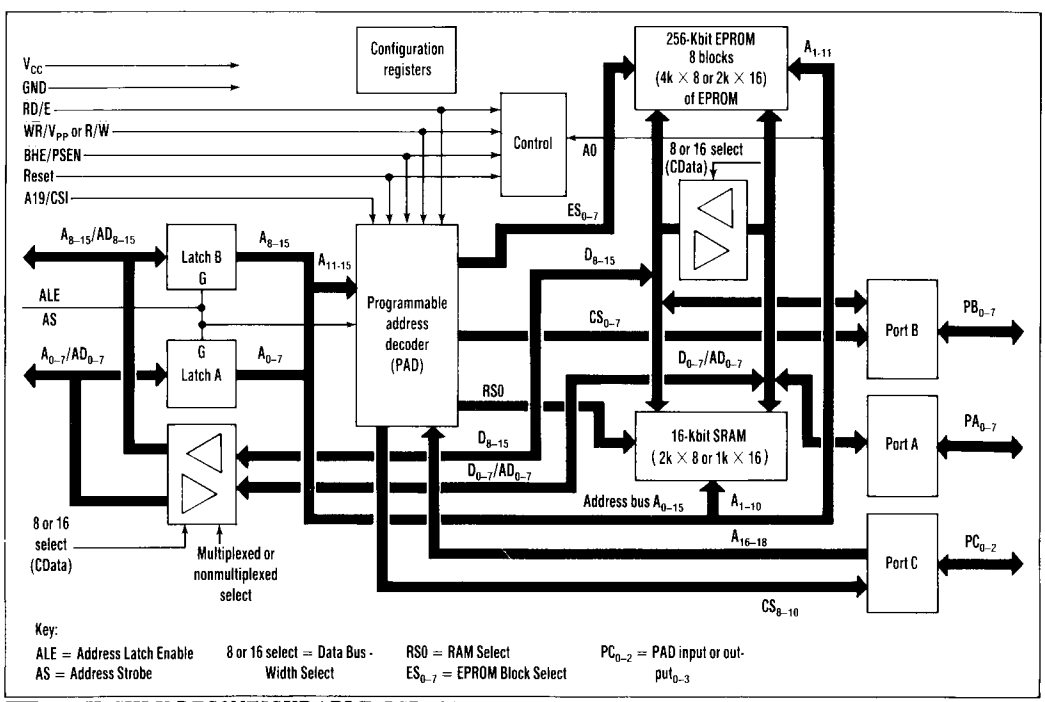
The **PSD301** is designed to adapt the characteristics of different microcontrollers to an embedded-control design. The PAD plays a major role in this function. It performs similarly to a small programmable array logic (PAL) device. The PAD has up to 13 inputs and 11 outputs in a NOR-gate array, and it can implement up to four sum-of-product expressions based on address inputs, control signals, and chip-select inputs. The PAD selects all of the chip's internal parts, and generates external chip selects with a 35-ns delay.

Address inputs from the host microcontroller are first fed to the 301's input latches, which stabilize the inputs when the device accesses memory in the multiplexed mode. The latches are made transparent in the nonmultiplexed mode. Five low-order address inputs and five programmable control lines are fixed functions; the Address-Latch-Enable and Reset lines have programmable polarity. The high-order address lines can be either address or general-purpose inputs for logic functions.

For more efficient use of memory space, internal and external PAD-Select signals can override EPROM memory with overlapping addresses. Therefore, if all of the EPROM isn't used for program storage, the unused space can be allocated to I/O ports, static RAM, or other PAD-select signals.

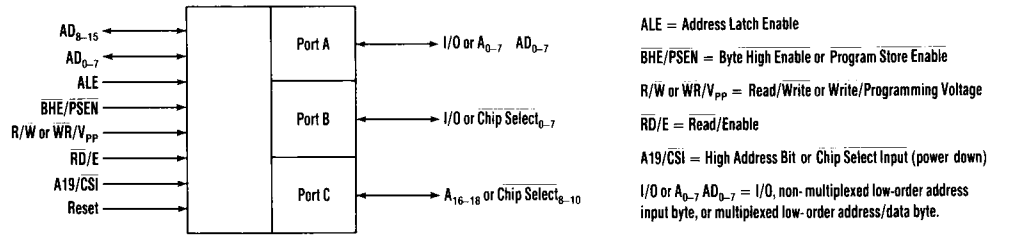
The EPROM is configurable as 32 kwords by 8 bits, or 16 kwords by 16 bits, and it's partitioned into eight equal mappable blocks with a resolution of 4 kbytes or 2 kwords. Access time, including PAD decoding time, is 120 ns. The configuration registers also consist of EPROM cells. The registers store the programmed configuration bits that make it possible for users to set the device, I/O, and control functions according to the required operating mode. The 16-kbit 120-ns static RAM is configurable as 2 kwords by 8 bits, or 1 kword by 16 bits. The memory blocks can be noncontiguously mapped over the addressable range of 1 Mbyte or 0.5 Mwords. Consequently, programmers can scramble the code to prevent direct copying.

I/O ports A and B in the 8- and 16-



1. A HIGHLY RECONFIGURABLE PSD301 microcontroller peripheral from WaferScale Integration has multiplexed or nonmultiplexed data and address buses with selectable 8- or 16-bit bus widths. The programmable address decoder (PAD) helps supply up to 45 configuration options for supporting a range of 8- and 16-bit microcontrollers.

USER-CONFIGURABLE MICROCONTROLLER INTERFACE



2. I/O PORT CONFIGURATION FOR THE PSD301 IS PROGRAMMED by signals from the PAD, which are derived partly from programmed bits in the configuration registers. The three ports configured for multiplexed address and data with a 16-bit wide data bus are shown.

bit configurations are data ports in the nonmultiplexed mode, and both ports can be configured as either data or address ports in the multiplexed mode *(Fig. 2)*. Port C is independent of any configuration—it can supply multiple chip-select outputs or serve as address inputs.

The default configuration of port A in the nonmultiplexed address/data mode sets the port to deliver I/O lines. In this mode, each pin can be set as an input or output and can have a CMOS or open-drain output. Alternatively, each bit of port A can be configured as a low-order latched-address-bus bit to access external peripherals or memory that requires several low-order lines. Another option in this mode sets the entire port to track the low-order address/data multiplexed bus. This feature links the host microcontroller to shared resources without the use of external buffers and decoders.

In the nonmultiplexed mode, port A becomes the chip's low-order data-bus byte. When a read operation is executed from an internal 301 location, data is directed out on port A pins. When a write cycle is executed into an internal 301 location, data is driven into port A.

The operation of port B in the multiplexed address/data and 8-bit nonmultiplexed modes is the same as port A. However, as an alternative, each bit can be configured to supply a Chip-Select Output signal from the PAD. In the 16-bit nonmultiplexed mode, port B is the high-order data-bus byte of the chip. When a read operation is executed from an internal high-order data-bus byte location, the data appears on port B pins. When a write operation is executed into an internal high-order data-bus byte location, data and write operation signals are present at port B.

Each pin of port C in all modes can be configured as an input or output from the PAD. Although designated as high-order address bus pins, they can be used for any logic inputs to the PAD or for external chip-select outputs from the PAD.

With this degree of operational flexibility, the 301 can team up with all popular 8- and 16-bit microcontrollers from such companies as Advanced Micro Devices, Intel, Motorola, National Semiconductor, Texas Instruments, and Zilog. For example, the polarity of the 301's control signals can be programmed for direct connection of the read-write and output enable pins of the 68HCXX microcontroller family. The 16-bit configuration can boost the performance of 16-bit controllers, such as the 80186, 8096, 80196, 16000, and others, without adding external devices. And the 8051 microcontroller family can extend its memory space by using the separate address and program memory space of the 301. The 301 is cascadable for increased width or depth for multiplexed byte- or word-wide embedded-control designs.

In the standby mode, commercial versions of the 301 draw 150 μA and 1.5 mA for CMOS and TTL interfaces, respectively. Active current for CMOS interfaces with or without selected memory blocks, or with the EPROM blocks selected, is 55 mA. That level increases to 80 mA for TTL interfaces. Selecting the static RAM block increases active current to 105 mA and 130 mA for CMOS and TTL, respectively.

WaferScale Integration houses the device in a 44-pin surface-mounted package to meet the form-factor requirements of such products as 5.25-, 3.5-, and 2.5-in. disk drives, cellular phones, and modems. System development tools include an IBM-PC plug-in programmer board and remote socket adaptor. They also contain a software development package that runs on an IBM PC/XT/AT or compatible computer with a MS-DOS version 3.1 or higher, 640 kbytes of RAM, and a hard disk.□

PRICE AND AVAILABILITY

The commercial version of the PSD301, packaged in a 44-pin plastic leaded chip carrier, is priced at $15 each in quantities of 1000. Military parts are also available. Other package options are ceramic leaded chip carriers and pin grid array packages with windows. The PSD301 is being sampled now, with production quantities available in January, 1990.

WaferScale Integration Inc., 47280 Kato Rd., Fremont, CA 94538; (415) 656-5400.

WSI

WAFERSCALE INTEGRATION, INC.

PROGRAMMABLE PERIPHERALS

SINGLE-CHIP CMOS USER-CONFIGURABLE PERIPHERAL WITH MEMORY – COMMERCIAL & MILITARY

Part No.	Description	Speed (ns) Comm'l	Speed (ns) Military	Availability Samples	Availability Prodn	Package Selection J	L	Q	X
PSD301	Programmable Microcontroller Peripherals with Memory; x8/x16; 256Kb – 1Mb EPROM; 16K SRAM; PAD; System Features.	120		NOW	Q4 '91	•	•	•	
		150-200		NOW	NOW	•	•	•	•
			200		NOW		•		•
PSD311		120		NOW	Q4 '91	•	•	•	
		150-200		NOW	Q4 '91	•	•	•	•
			200		Q4 '91		•		•
PSD302		120		NOW	Q1 '92	•	•		
		150-200		NOW	Q1 '92	•	•		
PSD312		120		NOW	Q1 '92	•	•		
		150-200		NOW	Q1 '92	•	•		
PSD303		120		Q4 '91	Q1 '92				
		150-200		Q4 '91	Q1 '92				
PSD313		120		Q4 '91	Q1 '92				
		150-200		Q4 '91	Q1 '92				
MAP168	DSP Peripheral with Memory. Features: 128K Bits EPROM, 32K Bits SRAM Programmable Address Decoder (PAD) Configurable: x8 or x16.	45-55		NOW	NOW	•	•	•	•
			55		NOW	•		•	

HIGH-PERFORMANCE CMOS USER-CONFIGURABLE EMBEDDED CONTROLLER – COMMERCIAL & MILITARY

Part No.	Description	Speed (ns) Comm'l	Speed (ns) Military	Availability Samples	Availability Prodn	Package Selection Q	X
PAC1000	Programmable Peripheral Controller optimized for High-Performance Control Systems. Key Features Include: 16-Bit CPU, 16-Bit Address Port, 16-Bit Output Control, 8-Bit I/O Port and Configuration Registers.	12MHz		NOW	NOW	•	•
			12MHz	NOW	NOW		•
		16MHz		NOW	NOW	•	•

HIGH-PERFORMANCE CMOS USER-CONFIGURABLE MICROSEQUENCER/STATE MACHINE – COMMERCIAL & MILITARY

Part No.	Description	Speed (ns) Comm'l	Speed (ns) Military	Availability Samples	Availability Prodn	Package Selection J	L	S	T
SAM448	User-Programmable Microsequencer for Implementing High-Performance State Machines. Includes EPROM integrated with Branch Control Logic, Pipeline Register, Stack and Loop Counter and 768 Product Terms.	20-25MHz		NOW	NOW	*	•	*	•
			20MHz	NOW	NOW		•		•

*J and S packages not available in 30MHz

SOFTWARE DEVELOPMENT TOOLS †

Part No.	Includes	Availability
PSD - GOLD	Contains PSD301/MAP168 Software, Users Manual, WS6000 MagicPro (PC Based Programmer), WS6014(J/L) or WS6015(X) Adapter and 2 Sample Devices	NOW
PSD - SILVER	Contains PSD301/MAP168 Software and Users Manual	NOW
PAC1000 - GOLD	Contains PAC1000 Software, Users Manual, WS6000 MagicPro (PC Based Programmer), WS6010 (X) Adapter and 2 Sample Devices	NOW
PAC1000 - SILVER	Contains PAC1000 Software and Users Manual	NOW
SAM448 - GOLD	Contains SAM448 Software, Users Manual, WS6000 MagicPro (PC Based Programmer), WS6008(T) or 6009(C,J,L) Adapter and 2 Sample Devices	NOW
SAM448 - SILVER	Contains SAM448 Software and Users Manual	NOW
MEMORY - SILVER††	Contains WSI EPROM/RPROM Programming Software and Users Manual	NOW

† 1) All Development Systems include: 12 Month Software Update Service, access to WSI's 24 Hour Electronic Bulletin Board.
2) Package adaptor must be specified when ordering any "Gold" system.

†† 1) Memory-Silver is included in all development systems.

NON-VOLATILE MEMORY

CMOS PROMs – COMMERCIAL

Part No.	Architecture	Description	Speed (ns)	Package Selection D	J	L	P	S	T
WS57C191B	2K x 8	16K CMOS PROM	35-55	•	•		•		
WS57C291B	2K x 8	16K CMOS PROM	35-55					•	•
WS57C45	2K x 8	16K CMOS Reg. PROM	25-35					•	•
WS57C43B	4K x 8	32K CMOS PROM	35-70	•	•			•	•
WS57C49B	8K x 8	64K CMOS PROM	35-70	•	•			•	•
WS57C49C	8K x 8	64K CMOS PROM	35-70	•	•			•	•
WS57C51C	16K x 8	128K CMOS PROM	35-70	•	•	•			•
WS57C71C	32K x 8	256K CMOS PROM	45-70	•	•	•			•

CMOS PROMs – MILITARY

Part No.	Architecture	Description	Speed (ns)	DESC SMD	Package Selection C	D	F	H	K	T	Z
WS57C191B	2K x 8	16K CMOS PROM	45-55	•	•	•	•				•
WS57C291B	2K x 8	16K CMOS PROM	45-55	•					•	•	
WS57C45	2K x 8	16K CMOS Reg. PROM	35-45	•	•		•	•	•	•	
WS57C43B	4K x 8	32K CMOS PROM	45-70		•					•	
WS57C49B	8K x 8	64K CMOS PROM	45-70	•	•	•	•			•	
WS57C49C	8K x 8	64K CMOS PROM	45-70	•	•	•	•			•	
WS57C51C	16K x 8	128K CMOS PROM	45-70		•	•				•	
WS57C71C	32K x 8	256K CMOS PROM	55-70		•	•				•	

NON-VOLATILE MEMORY (Cont.)

HIGH-SPEED CMOS EPROMs – COMMERCIAL

Part No.	Architecture	Description	Speed (ns)	Package Selection D	J	L	T
WS57C64F	8K x 8	High-Speed 64K CMOS EPROM	55-70	•	•		
WS57C128F	16K x 8	High-Speed 128K CMOS EPROM	55-70	•			
WS57C128FB	16K x 8	High-Speed 128K CMOS EPROM	35-45	•	•	•	
WS57C256F	32K x 8	High-Speed 256K CMOS EPROM	45-70	•	•	•	•

HIGH-SPEED CMOS EPROMs – MILITARY

Part No.	Architecture	Description	Speed (ns)	DESC SMD	Package Selection C	D	T	L
WS57C64F	8K x 8	High-Speed 64K CMOS EPROM	70	•	•	•		
WS27C64F	8K x 8	Low-Power 64K CMOS EPROM	90	•	•	•		
WS57C128F	16K x 8	High-Speed 128K CMOS EPROM	70	•	•	•		
WS57C128FB	16K x 8	High-Speed 128K CMOS EPROM	45-55		•	•		
WS27C128F	16K x 8	Low-Power 128K CMOS EPROM	90	•	•	•		
WS57C256F	32K x 8	High-Speed 256K CMOS EPROM	55-70	•	•	•	•	
WS27C256F	32K x 8	Low-Power 256K CMOS EPROM	90	•	•	•		•

CMOS EPROMs – COMMERCIAL

Part No.	Architecture	Description	Speed (ns)	Package Selection D	J	L
WS27C010L	128K x 8	Low-Power 1 Meg CMOS EPROM	120-150	•	•	•
WS27C210L	64K x 16	Low-Power 1 Meg CMOS EPROM	100-200	•	•	•

CMOS EPROMs – MILITARY

Part No.	Architecture	Description	Speed (ns)	DESC SMD	Package Selection C	D	L	T
WS27C256L	32K x 8	Low-Power 256K CMOS EPROM	120-250	•	•	•		•
WS27C512L	64K x 8	Low-Power 512K CMOS EPROM	120-200	•	•	•		•
WS27C010L	128K x 8	Low-Power 1 Meg CMOS EPROM	150-200	•	•	•	•	
WS27C210L	64K x 16	Low-Power 1 Meg CMOS EPROM	150-200		•	•	•	

CMOS BIT SLICE AND LOGIC

Part No.	Description	Speed		Package Selection							
		Comm'l	Military	B	G	J	K	L	P	S	Y
WS5901	4-Bit CMOS Bit Slice Processor	32,43 MHz	32,43MHz						•		•
WS59016	16-Bit CMOS Bit Slice Processor	15 MHz	12.5MHz	•		•		•			
WS59032	32-Bit CMOS Bit Slice Processor	26.4,33 MHz	23.6,29 MHz		•						
WS5910	CMOS Microprogram Controller	20,30 MHz	20,30 MHz						•		•
WS59510	16K x 16 CMOS Multiplier-Accum.	30-50 ns			•	•			•		
WS59520	CMOS Pipeline Register	Tpd = 22ns	Tpd = 24ns				•			•	
WS59521	CMOS Pipeline Register	Tpd = 22ns	Tpd = 24ns				•			•	
WS59820	CMOS Bi-Directional Register	Tpd = 23ns	Tpd = 25ns		•	•					

WSI PACKAGE DESCRIPTIONS

Package Code	Description	Window	Surface Mount	Plastic/OTP
B/R	Ceramic Sidebrazed Dip	N/Y	N	–
C	Ceramic Leadess Chip Carrier (CLLCC)	Y	Y	–
C/Z	Ceramic Leadless Chip Carrier (CLLCC)	Y/N	Y	–
D/Y	0.600" Ceramic Dip	Y/N	N	–
F/H	Ceramic Flatpack	Y/N	Y	–
J	Plastic Leaded Chip Carrier (PLDCC)	N	Y	Y
L/N	Ceramic Leaded Chip Carrier (CLDCC)	Y/N	Y	–
P	Plastic Dip	N	N	Y
Q	Plastic Quad Flat Pack (PQFP)	N	Y	Y
S	0.300" Plastic Dip	N	N	Y
T/K	0.300" Ceramic Dip	Y/N	N	–
X/G	Ceramic Pin Grid Array (CPGA)	Y/N	N	–

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Ordering Information
High-Performance CMOS Products

PSD3XX **-35** **D** **I** **B**

Basic Part Number

Manufacturing Process:

(Blank) = WSI Standard Manufacturing Flow

B = MIL-STD-883C Manufacturing Flow

Operating Temperature Range:

(Blank) = Commercial: 0° to +70°C
V_{CC}: +5V ± 5%

I = Industrial: −40° to +85°C
V_{CC}: +5V ± 10%

M = Military: −55° to +125°C
V_{CC}: +5V ± 10%

Package:

		Window
A	= PPGA Plastic Pin Grid Array	No
B	= 0.900″ Size Brazed Ceramic DIP	No
C	= CLLCC Ceramic Leadless Chip Carrier	Yes*
D	= 0.600″ CERDIP	Yes
F	= Ceramic Flatpack	Yes*
G	= CPGA Ceramic Pin Grid Array	No
H	= Ceramic Flatpack	No*
J	= Plastic Leaded Chip Carrier	No*
K	= 0.300″ Thin CERDIP	No
L	= CLDCC Ceramic Leaded Chip Carrier	Yes*
N	= CLDCC Ceramic Leaded Chip Carrier	No*
P	= 0.600″ Plastic DIP	No
Q	= Plastic Quad Flatpack	No*
R	= Ceramic Side Brazed	Yes
S	= 0.300″ Thin Plastic DIP	No
T	= 0.300″ Thin CERDIP	Yes
W	= Waffle Packed Dice	—
X	= Ceramic Pin Grid Array	Yes
Y	= 0.600″ CERDIP	No
Z	= CLLCC	No

Speed:

−120 = 120 ns
−150 = 150 ns
−200 = 200 ns
Etc.

*Surface Mount

Section Index

Programmable Peripheral

PSD301

Programmable Microcontroller Peripheral with Memory

Key Features

- ❑ Single Chip Programmable Peripheral for Microcontroller-based Applications
- ❑ 19 Individually Configurable I/O pins that can be used as
  - — Microcontroller I/O port expansion
  - — Programmable Address Decoder (PAD) I/O
  - — Latched address output
  - — Open drain or CMOS
- ❑ Two Programmable Arrays (PAD A and PAD B)
  - — Total of 40 Product Terms and up to 16 Inputs and 24 Outputs
  - — Address Decoding up to 1 MB
  - — Logic replacement
- ❑ "No Glue" Microcontroller Chip-Set
  - — Built-in address latches for multiplexed address/data bus
  - — Non-multiplexed address/data bus mode
  - — Selectable 8 or 16 bit data bus width
  - — ALE and Reset polarity programmable
  - — Selectable modes for read and write control bus as $\overline{RD}/\overline{WR}$ or R/$\overline{W}$/E
  - — BHE/pin for byte select in 16-bit mode
  - — PSEN/pin for 8051 users
- ❑ 256 Kbits of UV EPROM
  - — Configurable as 32K x 8 or as 16K x 16
  - — Divides into 8 equal mappable blocks for optimized mapping
  - — Block resolution is 4K x 8 or 2K x 16
  - — 120 ns EPROM access time, including input latches and PAD address decoding.
- ❑ 16 Kbit Static RAM
  - — Configurable as 2K x 8 or as 1K x 16
  - — 120 ns SRAM access time, including input latches and PAD address decoding
- ❑ Address/Data Track Mode
  - — Enables easy Interface to Shared Resources (Mail Box SRAM) with other Microcontrollers or a Host Processor
- ❑ Built-In Security
  - — Locks the PSD301 Configuration and PAD Decoding
- ❑ Available in a Variety of Packaging
  - — 44 Pin PLDCC and CLDCC
  - — 52 Pin PQFP
  - — 44 Pin CPGA
- ❑ Simple Menu-Driven Software: Configure the PSD301 on an IBM PC
- ❑ Pin Compatible with the PSD3XX Family

Partial Listing of Microcontrollers Supported

- ❑ **Motorola family:** M6805, M68HC11, M68HC16, M68000/10/20, M60008, M683XX
- ❑ **Intel family:** 8031/8051, 8096/8098, 80186/88, 80196/98
- ❑ **TI:** TMS320C14
- ❑ **Signetics:** SC80C451, SC80552
- ❑ **Zilog:** Z8, Z80, Z180
- ❑ **National:** HPC16000, HPC63400

Applications

- ❑ Computers (Workstations and PCs)
  - — Fixed Disk Control, Modem, Imaging, Laser Printer Control
- ❑ Telecommunications
  - — Modem, Cellular Phone, Digital PBX, Digital Speech, FAX, Digital Signal Processing
- ❑ Industrial
  - — Robotics, Power Line Access, Power Line Motor
- ❑ Medical Instrumentation
  - — Hearing Aids, Monitoring Equipment, Diagnostic Tools
- ❑ Military
  - — Missile Guidance, Radar, Sonar, Secure Communications, RF Modems

Introduction

The PSD301 is a member of the rapidly growing family of PSD devices. The PSD301 is ideal for microcontroller-based applications, where fast time-to-market, small form factor, and low power consumptions are essential. When combined in an 8- or 16-bit system, virtually any microcontroller (68HC11, 8051, 8096, 16000, etc.) and the PSD301 work together to create a very powerful chip-set solution. This implementation provides all the required control and peripheral elements of a microcontroller-based system peripheral with no external discrete "glue" logic required.

The solution comes complete with simple system software development tools for integrating the PSD301 with the microcontroller. Hosted on the IBM PC platforms or compatibles, the easy to use software enables the designer complete freedom in designing the system.

Product Description

The PSD301 integrates high performance user-configurable blocks of EPROM, SRAM, and programmable logic technology to provide a single chip microcontroller interface. The major functional blocks include two programmable logic arrays, PAD A and PAD B, 256K bits of high speed EPROM, 16K bits of high speed SRAM, input latches, and output ports. The PSD301 is ideal for applications requiring high performance, low power, and very small form factors. These include fixed disk control, modem, cellular telephone, instrumentation, computer peripherals, military and similar applications.

The PSD301 offers a unique single-chip solution for microcontrollers that need:

- ❑ I/O reconstruction (microcontrollers lose at least two I/O ports when accessing external resources).
- ❑ More EPROM and SRAM than the microcontroller's internal memory.
- ❑ Chip-select, control, or latched address lines that are otherwise implemented discretely.
- ❑ An interface to shared external resources.

WSI's PSD301 (shown in Figure 1) can efficiently interface with, and enhance, any 8- or 16-bit microcontroller system. This is the first solution that provides microcontrollers with port expansion, latched addresses, two programmable logic arrays PAD A and PAD B, an interface to shared resources, 256K bit EPROM, and 16K bit SRAM on a single chip. The PSD301 does not require any glue logic for interfacing to any 8- or 16-bit microcontroller.

The 8051 microcontroller family can take full advantage of the PSD301's separate program and data address spaces. Users of the 68HCXX family of microcontrollers can change the functionality of the control signals and directly connect the R/$\overline{W}$ and E, or the R/$\overline{W}$ and $\overline{DS}$ signals. Users of 16-bit microcontrollers (including the 80186, 8096, 80196, 16XXX) can use the PSD301 in a 16-bit configuration. Address and data buses can be configured to be separate or multiplexed, whichever is required by the host processor.

Product Discription (Cont.)

The flexibility of the PSD301 I/O ports permits interfacing to shared resources. The arbitration can be controlled internally by PAD A outputs. The user can assign the following functions to these ports: standard I/O pins, chip-select outputs from the PAD A and PAD B, or latched address or multiplexed low-order address/data byte. This enables users to design add-on systems such as disk drives, modems, etc., that easily interface to the host bus (e.g., IBM PC, SCSI).

The PSD301 on-chip programmable address decoder (PAD A) enables the user to map the I/O ports, eight segments of EPROM (as 4K x 8 or as 2K x 16) and SRAM (as 2K x 8 or as 1K x 16) anywhere in the address space of the microcontroller. PAD B can implement up to 4 sum-of-product expressions based on address inputs and control signals.

Figure 1. PSD301 Architecture

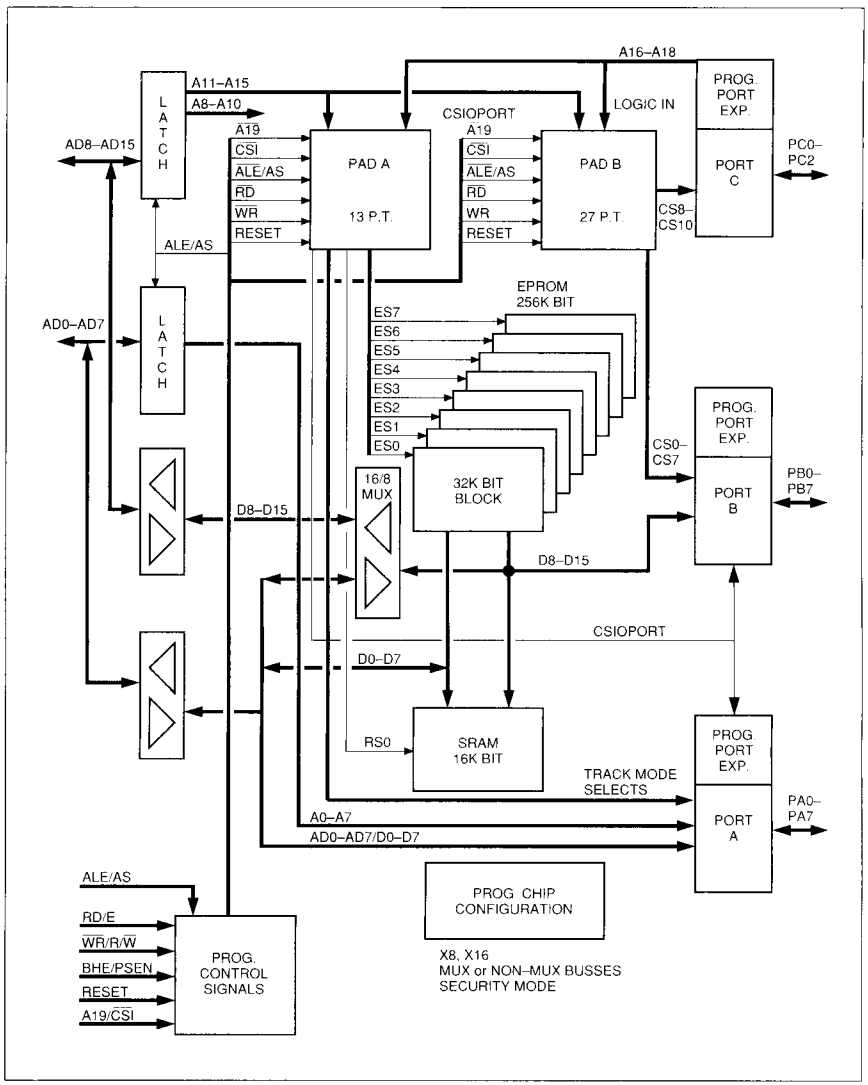
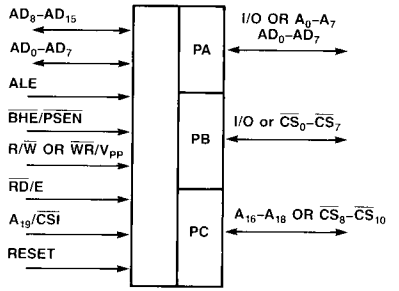
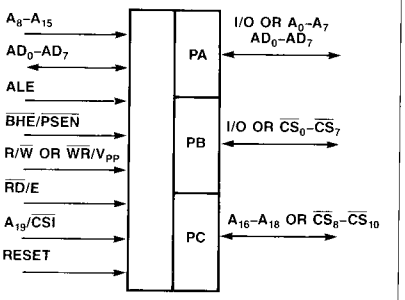


Figure 2. PSD301 Port Configurations

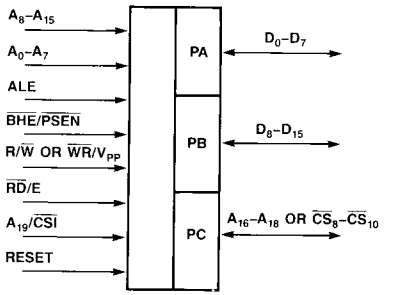
Figure 2 shows the PSD301's I/O port configurations.



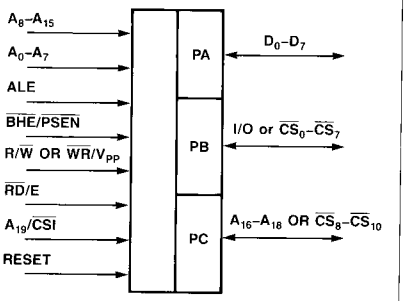
PSD301 configured for multiplexed 16-bit address/data bus



PSD301 configured for multiplexed 8-bit address/data bus.



PSD301 configured for non-multiplexed 16-bit address/data bus.



PSD301 configured for non-multiplexed 8-bit address/data bus.

Legend:

AD_0–AD_7 = addresses A_0–A_7 multiplexed with data lines D_0–D_7.
AD_8–AD_{15} = addresses A_8–A_{15} multiplexed with data lines D_8–D_{15}.

Table 1. PSD301 Pin Descriptions

Name	Type	Description
$\overline{BHE}/\overline{PSEN}$	I	When the data bus width is 8 bits (CDATA = 0), this pin is $\overline{PSEN}$. In this mode, $\overline{PSEN}$ is the active low EPROM read pulse. The SRAM and I/O ports read signal is generated when $\overline{RD}$ is low (CRRWR = 0), or when E and R/$\overline{W}$ are high (CRRWR = 1). If the host processor is a member of the 8031 family, $\overline{PSEN}$ must be connected to the corresponding host pin. In other 8-bit host processors that do not have a special EPROM-only read strobe, $\overline{PSEN}$ should be tied to V_{CC}. In this case, $\overline{RD}$ or E and R/$\overline{W}$ provide the read strobe for the SRAM, I/O ports, and EPROM. When the data bus width is configured as 16 (CDATA = 1), this pin is $\overline{BHE}$. When $\overline{BHE}$ is low, a high-order byte is read from, or written into the PSD301, depending on the operation being read or write, respectively. In programming mode, this pin is pulsed between V_{PP} and 0.
$\overline{WR}/V_{PP}$ or R/$\overline{W}/V_{PP}$	I	In the operating mode, this pin's function is $\overline{WR}$ (CRRWR = 0) or R/$\overline{W}$ (CRRWR = 1). When configured as $\overline{WR}$, a write operation is executed during an active low pulse. When configured as R/$\overline{W}$, with R/$\overline{W}$ = 1 and E = 1, a read operation is executed; if R/$\overline{W}$ = 0 and E = 1, a write operation is executed. In programming mode, this pin must be tied to V_{PP} voltage.
$\overline{RD}$/E	I	When configured as $\overline{RD}$ (CRRWR = 0), this pin provides an active low $\overline{RD}$ strobe. When configured as E (CRRWR = 1), this pin becomes an active high pulse, which, together with R/$\overline{W}$ defines the cycle type. Then, if R/$\overline{W}$ = 1 and E = 1, a read operation is executed. If R/$\overline{W}$ = 0 and E = 1, a write operation is executed.
$\overline{CSI}$/A19	I	This pin has two configurations. When it is $\overline{CSI}$ (CA19/$\overline{CSI}$ = 0) and the pin is asserted high, the device is deselected and powered down. (See Tables 12 and 13 for the chip state during power-down mode.) If the pin is asserted low, the chip is in normal operational mode. When it is A19, (CA19/$\overline{CSI}$ = 1), this pin can be used as an additional input to the PAD. In this mode, there is no power-down capability.
RESET	I	This user-programmable pin can be configured to reset on high level (CRESET = 1) or on low level (CRESET = 0). It should remain active for at least 100 ns. See Tables 10 and 11 for the chip state after reset.
ALE or AS	I	In the multiplexed modes, the ALE pin functions as an Address Latch Enable or as an Address strobe and can be configured as an active high or active low signal. The ALE or AS trailing edge latches lines AD15/A15–AD0/A0, A16–A19, and $\overline{BHE}$, depending on the PSD301 configuration. See Table 8. In the non-multiplexed modes, it can be used as a general-purpose PAD input signal.

Legend: The I/O column abbreviations are: I = input; I/O = input/output; P = power.

NOTE: 3. All the configuration bits mentioned in Table 1 appear in parentheses and are explained in the Configuration Register section.

Table 1. PSD301 Pin Descriptions (Cont.)

Name	Type	Description
PA7 PA6 PA5 PA4 PA3 PA2 PA1 PA0	I/O	PA7–PA0 is an 8-bit port that can be configured to track AD7/A7–AD0/A0 from the input (CPAF2 = 1). Otherwise (CPAF2 = 0), each bit can be configured separately as an I/O or lower-order latched address line. When configured as an I/O (CPAF1 = 0), the direction of the pin is defined by its direction bit, which resides in the direction register. If a pin is an I/O output, its data bit (which resides in the data register) comes out. When it is configured as a low-order address line (CPAF1 =1), A7–A0 can be made the corresponding output through this port (e.g., PA6 can be configured to be the A6 address line). Each port bit can be a CMOS output (CPACOD = 0) or an open drain output (CPACOD = 1). When the chip is in non-multiplexed mode (CADDRDAT = 0), the port becomes the data bus lines (D0–D7). See Figure 4.
PB7 PB6 PB5 PB4 PB3 PB2 PB1 PB0	I/O	PB7–PB0 is an 8-bit port for which each bit can be configured as an I/O (CPBF = 1) or chip-select output (CPBF = 0). Each port bit can be a CMOS output (CPBCOD = 0) or an open drain output (CPBCOD = 1). When configured as an I/O, the direction of the pin is defined by its direction bit, which resides in the direction register. If a pin is an I/O output, its data (which resides in the data register) comes out. When configured as a chip-select output, $\overline{CS0}$–$\overline{CS3}$ are a function of up to four product terms of the inputs to the PAD; $\overline{CS4}$–$\overline{CS7}$ then are each a function of up to two product terms. When the chip is in non-multiplexed mode (CADDRAT = 0) and the data bus width is 16 (CDATA = 1), the port becomes the most significant byte of the data bus (D8–D15). See Figure 6.
PC0 PC1 PC2	I/O	This is a 3-bit port for which each bit is configurable as a PAD input or output. When configured as an input (CPCF = 0), the bits can be latched with ALE (CADDHLT = 1) or be transparent inputs to the PAD (CADDHLT = 0). When a pin is configured as an output (CPCF = 1), it is a function of one product term of all PAD inputs. See Figure 7.
AD0/A0 AD1/A1 AD2/A2 AD3/A3 AD4/A4 AD5/A5 AD6/A6 AD7/A7	I/O	In multiplexed mode, these pins are the multiplexed low-order address/data byte. After ALE latches the addresses, these pins input or output data, depending on the settings of the $\overline{RD}$/E, $\overline{WR}$/V_{PP} or R/$\overline{W}$, and $\overline{BHE}$/$\overline{PSEN}$ pins. In non-multiplexed mode, these pins are the low-order address input byte.
AD8/A8 AD9/A9 AD10/A10 AD11/A11 AD12/A12 AD13/A13 AD14/A14 AD15/A15	I/O	In 16-bit multiplexed mode, these pins are the multiplexed high-order address/data byte. After ALE latches the addresses, these pins input or output data, depending on the settings of the $\overline{RD}$/E, $\overline{WR}$/V_{PP} or R/$\overline{W}$, and $\overline{BHE}$/$\overline{PSEN}$ pins. In all other modes, these pins are the high-order address input byte.
GND	P	V_{SS} (ground) pin.
V_{CC}	P	Supply voltage input.

Operating Modes

The PSD301's four operating modes allow it to interface directly to 8- and 16-bit microcontrollers and microprocessors with multiplexed and non-multiplexed address/data buses. These operating modes are:

- Multiplexed 8-bit address/data bus
- Multiplexed 16-bit address/data bus
- Non-multiplexed address/data, 8-bit data bus
- Non-multiplexed 16-bit address/data bus

Multiplexed 8-Bit Address/Data Bus

This mode is used to interface to microcontrollers with an 8-bit data bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is bi-directional and permits the latching of the address when the ALE signal is active. On the same pins, the data is read from or written to the device; this depends on the state of the $\overline{RD}$/E, $\overline{BHE}$/$\overline{PSEN}$, and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins. The high-order address/data bus (AD8/A8–AD15/A15) contains the high-order address bus byte. Ports A and B can be configured as in Table 2.

Multiplexed 16-Bit Address/Data Bus

This mode is used to interface to microcontrollers with a 16-bit data bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is bi-directional and permits the latching of the address when the ALE signal is active. On the same pins, the data is read from or written to the device; this depends on the state of the $\overline{RD}$/E, $\overline{BHE}$/$\overline{PSEN}$, and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins. The high-order address/data bus (AD8/A8–AD15/A15) is bi-directional and permits latching of the high-order address when the ALE signal is active on the same pins. The high-order data bus is read from or written to the device, depending on the state of the $\overline{RD}$/E, $\overline{BHE}$/$\overline{PSEN}$, and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins. Ports A and B can be configured as in Table 2.

Non-Multiplexed Address/Data, 8-Bit Data Bus

This mode is used to interface to non-multiplexed 8-bit microcontrollers with an 8-bit data bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is the low-order address input bus. The high-order address/data bus (AD8/A8–AD15/A15) is the high-order address bus byte. Port A is the low-order data bus. Port B can be configured as shown in Table 2.

Non-Multiplexed 16-Bit Address/Data Bus

This mode is used to interface to non-multiplexed 16-bit microcontrollers with a 16-bit data bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is the low-order address input bus. The high-order address/data bus (AD8/A8–AD15/A15) is the high-order address bus byte. Port A is the low-order data bus. Port B is the high-order data bus.

Table 2 summarizes the effect of the different operating modes on ports A, B, and the address/data pins. The configuration of Port C is independent of the four operating modes.

Table 2. PSD301 Bus and Port Configuration Options

	Multiplexed Address/Data	Non-Multiplexed Address/Data
8-Bit Data Bus		
Port A	I/O and/or low-order address lines or Low-order multiplexed address/data byte	D0–D7 data bus lines
Port B	I/O and/or $\overline{CS0}$–$\overline{CS7}$	I/O and/or $\overline{CS0}$–CS7
AD0/A0–AD7/A7	Low-order multiplexed address/data byte	Low-order address bus byte
AD8/A8–AD15/A15	High-order address bus byte	High-order address bus byte
16-Bit Data Bus		
Port A	I/O and/or low-order address lines or Low-order multiplexed address/data byte	Low-order data bus byte
Port B	I/O and/or $\overline{CS0}$–$\overline{CS7}$	High-order data bus byte
AD0/A0–AD7/A7	Low-order multiplexed address/data byte	Low-order address bus byte
AD8/A8–AD15/A15	High-order multiplexed address/data byte	High-order address bus byte

Programmable Address Decoder (PAD)

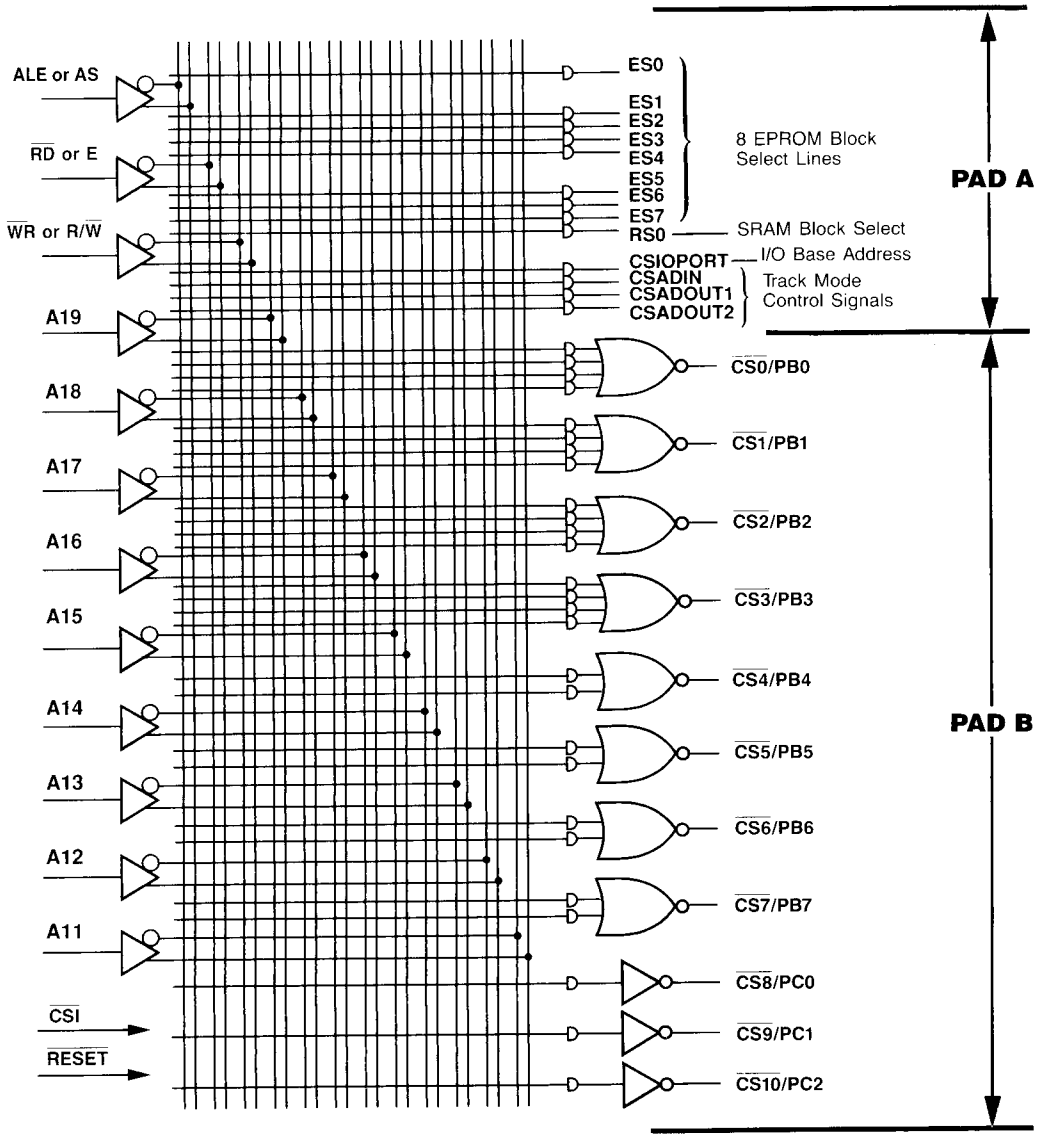
The PSD301 consists of two programmable arrays referred to as PAD A and PAD B (Figure 3). PAD A is used to generate chip select signals derived from the input address to the internal EPROM blocks, SRAM, I/O ports, and Track Mode signals. All its I/O functions are listed in Table 3 and shown in Figure 3. PAD B outputs to Ports B and C for off-chip usage.

PAD B can also be used to extend the decoding to select external devices or as a random logic replacement. The input bus to both PAD A and PAD B is the same. Using WSI's MAPLE software, each programmable bit in the PAD's array can have one of three logic states of 0, 1, and don't care (X). In a user's logic design, both PADs can share the same inputs using the X for input signals that are not supposed to affect other functions. The PADs use UV CMOS EPROM technology and can be programmed and erased by the user.

Table 3. PSD301 PAD A and B I/O Functions

	Function
PAD A and PAD B Inputs	
$\overline{CSI}$ or A19	In $\overline{CSI}$ mode (when high), PAD deselects all of its outputs and enters a power-down mode (see Tables 12 and 13). In A19 mode, it is another input to the PAD.
A16–A18	These are general purpose inputs from Port C. See Figure 3, Note 4.
A11–A15	These are address inputs.
$\overline{RD}$ or E	This is the read pulse or enable strobe input.
$\overline{WR}$ or R/$\overline{W}$	This is the write pulse or R/$\overline{W}$ select signal.
ALE	This is the ALE input to the chip.
RESET	This deselects all outputs from the PAD; it can not be used in product term equations. See Tables 10 and 11.
PAD A Outputs	
ES0–ES7	These are internal chip-selects to the 8 EPROM banks. Each bank can be located on any boundary that is a function of one product term of the PAD address inputs.
RS0	This is an internal chip-select to the SRAM. Its base address location is a function of one term of the PAD address inputs.
CSIOPORT	This internal chip-select selects the I/O ports. It can be placed on any boundary that is a function of one product term of the PAD inputs. See Tables 6 and 7.
CSADIN	This internal chip-select, when Port A is configured as a low-order address/data bus in the track mode (CPAF2 = 1), controls the input direction of Port A. CSADIN is gated externally to the PAD by the internal read signal. When CSADIN and a read operation are active, data presented on Port A flows out of AD0/A0–AD7/A7. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 5.
CSADOUT1	This internal chip-select, when Port A is configured as a low-order address/data bus in track mode (CPAF2 = 1), controls the output direction of Port A. CSADOUT1 is gated externally to the PAD by the ALE signal. When CSADOUT1 and the ALE signal are active, the address presented on AD0/A0–AD7/A7 flows out of Port A. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 5.
CSADOUT2	This internal chip-select, when Port A is configured as a low-order address/data bus in the track mode (CPAF2 = 1), controls the output direction of Port A. CSADOUT2 must include the write-cycle control signals as part of its product term. When CSADOUT2 is active, the data presented on AD0/A0–AD7/A7 flows out of Port A. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 5.
PAD B Outputs	
$\overline{CS0}$–$\overline{CS3}$	These chip-select outputs can be routed through Port B. Each of them is a function of up to four product terms of the PAD inputs.
$\overline{CS4}$–$\overline{CS7}$	These chip-select outputs can be routed through Port B. Each of them is a function of up to two product terms of the PAD inputs.
$\overline{CS8}$–$\overline{CS10}$	These chip-select outputs can be routed through Port C. See Figure 3, Note 4. Each of them is a function of one product term of the PAD inputs.

Figure 3. PSD301 PAD Description



Configuration Bits

The configuration bits shown in Table 4 are non-volatile cells that let the user set the device, I/O, and control functions to the proper operational mode. Table 5 lists all configuration bits. The configuration bits are programmed and verified during the programming phase. In operational mode, they are not accessible. To simplify implementing a specific mode, use the WSI's PSD301 MAPLE software to set the bits.

Table 4. PSD301 Non-Volatile Configuration Bits

Use This Bit	To
CDATA	Set the data bus width to 8 or 16 bits.
CADDRDAT	Set the address/data buses to multiplexed or non-multiplexed mode.
CRRWR	Set the $\overline{RD}$/E and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins to $\overline{RD}$ and $\overline{WR}$ pulse, or to E strobe and R/W status.
CA19/$\overline{CSI}$	Set A19/$\overline{CSI}$ to $\overline{CSI}$ (power-down) or A19 input.
CALE	Set the ALE polarity.
CPAF2	Set Port A either to track the low-order byte of the address/data multiplexed bus or to select the I/O or address option.[8]
CSECURITY	Set the security on or off.
CRESET	Set the RESET polarity.
$\overline{COMB}$/SEP	Set $\overline{PSEN}$ and $\overline{RD}$ for combined or separate address spaces (see Figures 8 and 9).
CPAF1	Configure each pin of Port A in multiplexed mode to be an I/O or address output.
CPACOD	Configure each pin of Port A as an open drain or active CMOS pull-up output.
CPBF	Configure each pin of Port B as an I/O or a chip-select output.
CPBCOD	Configure each pin of Port B as an open drain or active CMOS pull-up output.
CPCF	Configure each pin of Port C as an address input or a chip-select output.
CADDHLT	Configure pins A16–A19 to go through a latch or to have their latch transparent.
CATD	Configure pins A16–A19 as PAD logic inputs or high-order address inputs.

NOTE: 8. For functional and value descriptions, refer to table 5.

Table 5. PSD301 Configuration Bits (46 total bits)

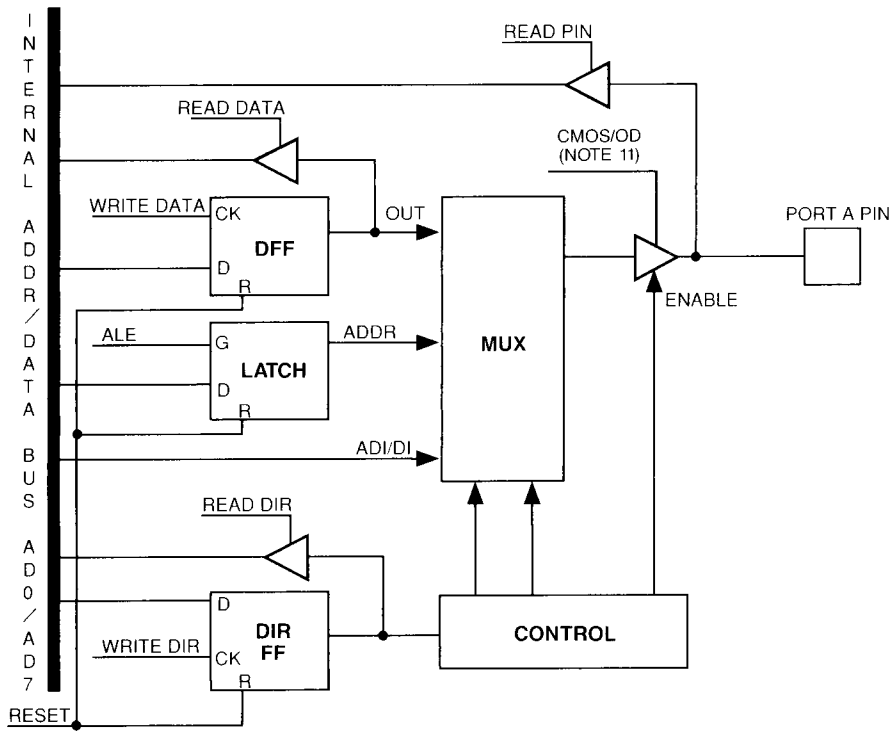
Configuration Bits	No. of Bits	Description
CDATA	1	8-bit or 16-bit data bus width CDATA = 0, 8-bit data bus CDATA = 1, 16 bit data bus
CADDRDAT	1	Address/data multiplexed or non-multiplexed (separate buses) CADDRDAT = 0, non-multiplexed address/data bus CADDRDAT = 1, multiplexed address/data bus
CRRWR	1	CRRWR = 0, $\overline{RD}$ and $\overline{WR}$ active low strobes CRRWR = 1, R/$\overline{W}$ status and E active high pulse
CA19/$\overline{CSI}$	1	A19 or $\overline{CSI}$ CA19/$\overline{CSI}$ = 0, enable power-down mode CA19/$\overline{CSI}$ = 1, A19 input to PAD
CALE	1	Active high or active low CALE = 0, active high CALE = 1, active low
CRESET	1	Active high or active low CRESET = 0, active low reset signal CRESET = 1, active high reset signal
$\overline{COMB}$/SEP	1	Combined or separate memory space for EPROM and SRAM $\overline{COMB}$/SEP = 0, combined $\overline{COMB}$/SEP = 1, separate
CPAF1	8	Port A I/Os or A0–A7 CPAF1 = 0, Port A pin = I/O CPAF1 = 1, Port A pin = Ai ($0 \leqslant i \leqslant 7$)
CPAF2	1	Port A AD0–AD7 (address/data multiplexed bus) CPAF2 = 0, address or I/O on Port A (according to CPAF1) CPAF2 = 1, address/data multiplexed on Port A (track mode)
CPBF	8	Port B I/Os or $\overline{CS0}$–$\overline{CS7}$ CPBF = 0, Port B Pin = $\overline{CSi}$ ($0 \leqslant i \leqslant 7$) CPBF = 1, Port B Pin = I/O
CPCF	3	Port C A16–A18 or $\overline{CS8}$–$\overline{CS10}$ CPCF = 0, Port C Pin = Ai ($16 \leqslant i \leqslant 18$) CPCF = 1, Port C Pin = $\overline{CSi}$ ($8 \leqslant i \leqslant 10$)
CPACOD	8	Port A CMOS or open-drain outputs CPACOD = 0, CMOS output CPACOD = 1, open-drain output
CPBCOD	8	Port B CMOS or open-drain outputs CPBCOD = 0, CMOS output CPBCOD = 1, open-drain output
CADDHLT	1	A16–A19 latched or latch transparent CADDHLT = 0, address latch transparent CADDHLT = 1, address latched (ALE dependent)
CATD	1	A16–A19 used as address or logic inputs CATD = 0, logic inputs CATD = 1, address inputs
CSECURITY	1	Security on or off CSECURITY = 0, no security CSECURITY = 1, secured part (cannot be copied)

NOTES: 9. WSI's MAPLE software will guide the user to the proper configuration choice.
10. In an unprogrammed or erased part, all configuration bits are 0.

Port Functions

The PSD301 has three I/O ports (Ports A, B, and C) that are configurable at the bit level. This permits great flexibility and a high degree of customization for specific applications. The following is a description of each port. Figure 4 shows the pin structure of Port A.

Figure 4. Port A Pin Structure



NOTE: 11. CMOS/OD determines whether the output is open drain or CMOS.

Port A in Multiplexed Address/Data Mode

The default configuration of Port A is I/O. In this mode, every pin can be set as an input or output by writing into the respective pin's direction flip flop (DIR FF, in Figure 4). As an output, the pin level can be controlled by writing into the respective pin's data flip flop (DFF, in Figure 4). When DIR FF = 1, the pin is configured as an output. When DIR FF = 0, the pin is configured as an input. The controller can read the DIR FF bits by accessing the READ DIR register; it can read the DFF bits by accessing the READ DATA register. Port A pin levels can be read by accessing the READ PIN register.

Individual pins can be configured as CMOS or open drain outputs. Open drain pins require external pull-up resistors. For addressing information, refer to Tables 6 and 7.

Alternatively, each bit of Port A can be configured as a low-order latched address bus bit. The address is provided by the port address latch, which latches the address on the trailing edge of ALE. PA0–PA7 can become A0–A7, respectively. This feature of the PSD301 lets the user generate low-order address bits to access external peripherals or memory that require several low-order address lines.

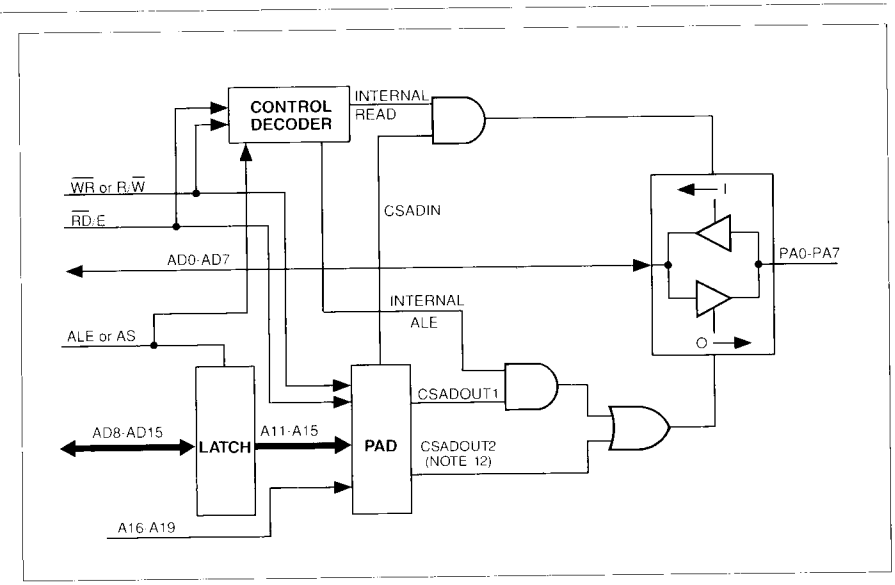
Port Functions (Cont.)

Another mode of Port A (CPAF2 = 1) sets the entire port to track the inputs AD0/A0–AD7/A7, depending on specific address ranges defined by the PAD's CSADIN, CSADOUT1, and CSADOUT2 signals. This feature lets the user interface the microcontroller to shared external resources without requiring external buffers and decoders. In this mode, the port is effectively a bi-directional buffer. The direction is controlled by using the input signals ALE, $\overline{RD}$/E, $\overline{WR}$/V_{PP} or R/$\overline{W}$, and the internal PAD outputs CSADOUT1, CSADOUT2 and CSADIN (see Figure 5). When CSADOUT1 and ALE are true, the address on the input AD0/A7–AD7/A7 pins flows out through Port A. (Carefully check the generation of CSADOUT1, and ensure that it is stable during the ALE pulse; see Figures 22 and 23). When CSADOUT2 is active, a write operation is performed (see note to Figure 5). The data on the input AD0/A7–AD7/A7 pins flows out through Port A. When CSADIN and a read operation is performed (depending on the mode of the $\overline{RD}$/E and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins), the data on Port A flows out through the AD0/A7–AD7/A7 pins. In this operational mode, Port A is tri-stated when none of the above-mentioned three conditions exist.

Port A in Non-Multiplexed Address/Data Mode

In this mode, Port A becomes the low order data bus byte of the chip. When reading an internal PSD301 location, data is presented on Port A pins. When writing to an internal PSD301 location, data present on Port A pins is written to that location.

Figure 5. Port A Track Mode



NOTE: 12. The expression for CSADOUT2 must include the following write operation cycle signals:
For CRRWR = 0, CSADOUT2 must include $\overline{WR}$ = 0.
For CRRWR = 1, CSADOUT2 must include E = 1 and R/$\overline{W}$ = 0.

Port B in Multiplexed Address/Data and in 8-Bit Non-Multiplexed Modes

The default configuration of Port B is I/O. In this mode, every pin can be set as an input or output by writing into the respective pin's direction flip flop (DIR FF, in Figure 6). As an output, the pin level can be controlled by writing into the respective pin's data flip flop (DFF, in Figure 6). When DIR FF = 1, the pin is configured as an output. When DIR FF = 0, the pin is configured as an input. The controller can read the DIR FF bits by accessing the READ DIR register; it can read the DFF bits by accessing the READ DATA register. Port B pin levels can be read by accessing the READ PIN register.

Port Functions (Cont.)

Individual pins can be configured as CMOS or open drain outputs. Open drain pins require external pull-up resistors. For addressing information, refer to Tables 6 and 7.

Alternatively, each bit of Port B can be configured to provide a chip-select output signal from the PAD. PB0–PB7 can provide $\overline{CS0}$–$\overline{CS7}$, respectively. Each of the signals $\overline{CS0}$–$\overline{CS3}$ is comprised of four product terms. Thus, up to four ANDed expressions can be ORed while deriving any of these signals. Each of the signals $\overline{CS4}$–$\overline{CS7}$ is comprised of two product terms. Thus, up to two ANDed expressions can be ORed while deriving any of these signals.

Port B in 16-Bit Non-Multiplexed Address/Data Mode

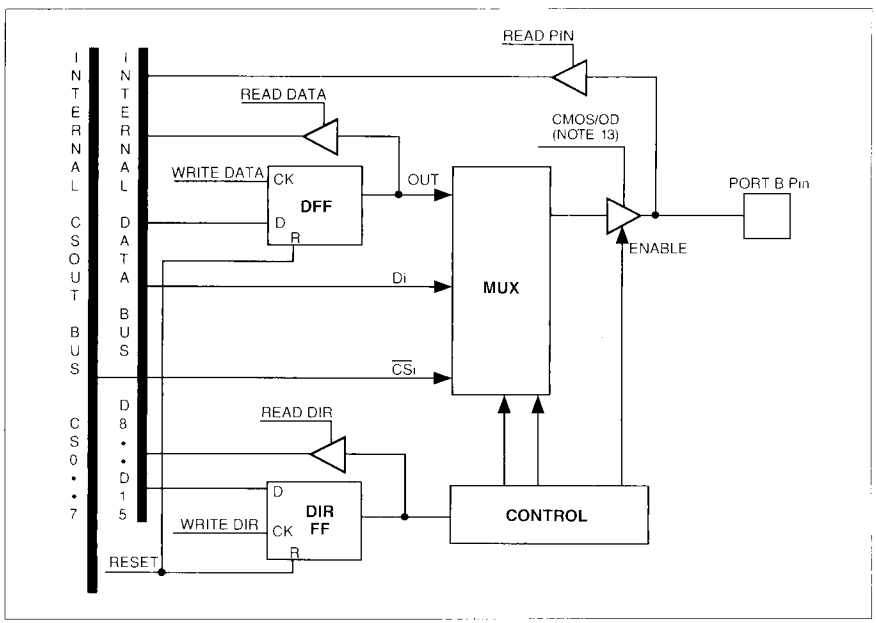
In this mode, Port B becomes the high-order data bus byte of the chip. When reading an internal PSD301 high-order data bus byte location, the data is presented on Port B pins. When writing to an internal PSD301 high-order data bus byte location, data present on Port B is written to that location. See Table 9.

Accessing the I/O Port Registers

Tables 6 and 7 show the offset values with the respect to the base address defined by the CSIOPORT. They let the user access the corresponding registers.

2

Figure 6. Port B Pin Structure



NOTE: 13. CMOS/OD determines whether the output is open drain or CMOS.

Table 6. I/O Port Addresses in an 8-bit Data Bus Mode

Register Name	Byte Size Access of the I/O Port Registers Offset from the CSIOPORT
Pin Register of Port A	+2 (accessible during read operation only)
Direction Register of Port A	+4
Data Register of Port A	+6
Pin Register of Port B	+3 (accessible during read operation only)
Direction Register of Port B	+5
Data Register of Port B	+7

Table 7. I/O Port Addresses in a 16-bit Data Bus Mode

Register Name	Word Size Access of the I/O Port Registers Offset from the CSIOPORT
Pin Register of Ports B and A	+2 (accessible during read operation only)
Direction Register of Ports B and A	+4
Data Register of Ports B and A	+6

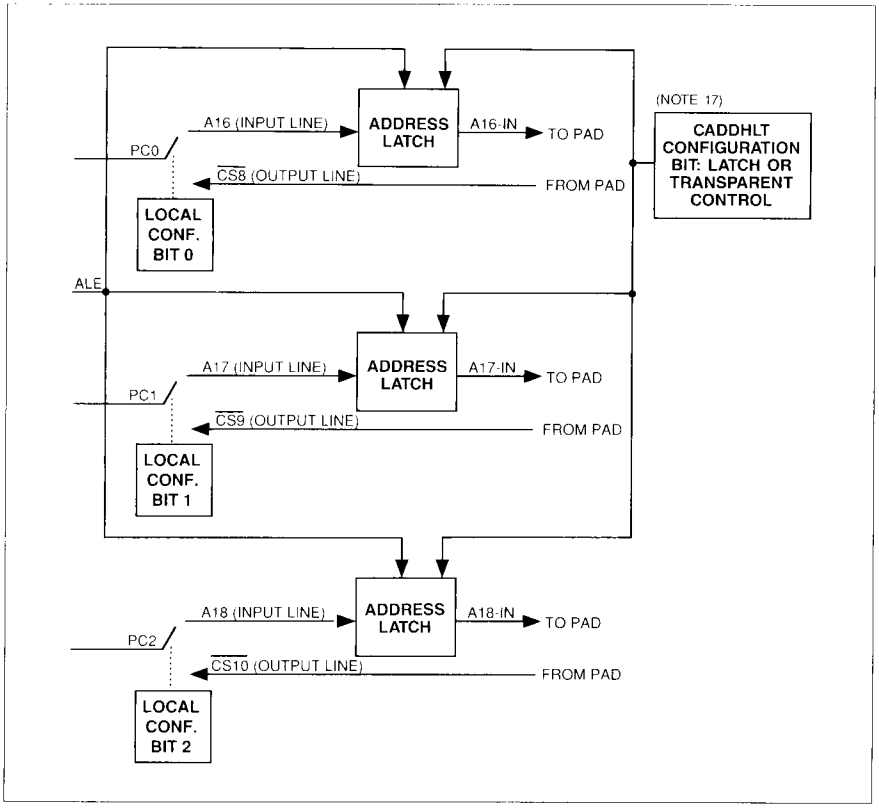
NOTES: 14. When the data bus width is 16, Port B registers can only be accessed if the $\overline{BHE}$ signal is low.
15. When accessing words, the high-order byte is connected to Port B, and the low-order byte is connected to Port A.
16. I/O Ports A and B are still byte-addressable, as shown in Table 6. For I/O Port B register access, $\overline{BHE}$ must be low.

Port C in All Modes

Each pin of Port C (shown in Figure 7) can be configured as an input or output from the PAD. As inputs, the pins are named A16–A18. Although the pins are given names of the high-order address bus, they can be used for any other logic inputs to the PAD. For example, A8–A10 can also be connected to those pins, reducing the boundaries of $\overline{CS0}$–$\overline{CS7}$ resolution to 256 bytes. Port C address latches can be programmed to latch the inputs by the trailing edge ALE or to be transparent.

Alternatively, PC0–PC2 can become $\overline{CS8}$–$\overline{CS10}$ outputs, respectively, providing the user with more external chip-select PAD outputs. Each of the signals $\overline{CS8}$–$\overline{CS10}$ is comprised of one product term.

Figure 7. Port C Structure



NOTE: 17. The CADDHLT configuration bit determines if A18–A16 are transparent via the latch, or if they must be latched by the trailing edge of the ALE strobe.

A16-A19 As Inputs

If one or more of the pins PC0, PC1, PC2 and CSI/A19 are configured as inputs, the configuration bits CADDHLT and CATD define their functionality inside the part. CADDHLT determines if these inputs are to be latched by the trailing edge of the ALE or AS signal (CADDHLT = 1), or enabled into the PSD301 at all times (CADDHLT = 0, transparent mode). CATD determines whether these lines are high-order address lines, that take part in the derivation of memory and I/O select signals inside the chip (CATD = 1), or logic input lines that have no impact on memory or I/O selections (CATD = 0). Logic input lines typically participate in the Boolean expressions implemented in the PAD.

EPROM

The PSD301 has 256K bits of EPROM. Depending on the configuration of the data bus, the EPROM can be organized as 32K x 8 (8-bit data bus) or as 16K x 16 (16-bit data bus). The EPROM has 8 banks of memory. Each bank can be placed in any address location by programming the PAD. Bank0–Bank7 can be selected by PAD outputs ES0–ES7, respectively. The EPROM banks are organized as 4K x 8 (8-bit data bus) or as 2K x 16 (16-bit data bus).

2

SRAM

The PSD301 has 16K bits of SRAM. Depending on the configuration of the data bus, the SRAM organization can be 2K x 8 (8-bit data bus) or 1K x 16 (16-bit data bus). The SRAM is selected by the RS0 output of the PAD.

Control Signals

The PSD301 control signals are $\overline{WR}/V_{PP}$ or R/$\overline{W}$, $\overline{RD}$/E, ALE, $\overline{BHE}/\overline{PSEN}$, Reset, and A19/$\overline{CSI}$. Each of these signals can be configured to meet the output control signal requirements of various microcontrollers.

$\overline{WR}/V_{PP}$ or R/$\overline{W}$

In operational mode, this signal can be configured as $\overline{WR}$ or R/$\overline{W}$. As $\overline{WR}$, all write operations to the PSD301 are activated by an active low signal on this pin. As R/$\overline{W}$, the pin works with the E strobe of the $\overline{RD}$/E pin. When R/$\overline{W}$ is high, an active high signal on the $\overline{RD}$/E pin performs a read operation. When R/$\overline{W}$ is low, an active high signal on the $\overline{RD}$/E pin performs a write operation.

$\overline{RD}$/E

In operational mode, this signal can be configured as $\overline{RD}$ or E. As $\overline{RD}$, all read operations to the PSD301 are activated by an active low signal on this pin. As E, the pin works with the R/$\overline{W}$ strobe of the $\overline{WR}/V_{PP}$ or R/$\overline{W}$ pin. When R/$\overline{W}$ is high, an active high signal on the $\overline{RD}$/E pin performs a read operation. When R/$\overline{W}$ is low, an active high signal on the $\overline{RD}$/E pin performs a write operation.

ALE or AS

ALE polarity is programmable. When programmed to be active high, a high on the pin causes the input address latches, Port A address latches, and Port C address latches to be transparent. The falling edge of ALE latches the information into the latches. When ALE is programmed to be active low, a low on the pin causes the input address latches, Port A address latches, Port C, and A19 address latches to be transparent. The rising edge of ALE latches the appropriate information into the latches. ALE is active only in the multiplexed modes.

$\overline{BHE}/\overline{PSEN}$

This pin's function depends on the PSD301 data bus width. If it is 8, the pin is $\overline{PSEN}$; if it is 16, the pin is $\overline{BHE}$. In 8-bit mode, the $\overline{PSEN}$ function lets the user work with two address spaces: program memory and data memory (if $\overline{COMB}$/SEP = 1). In this mode, an active low signal on the $\overline{PSEN}$ pin causes the EPROM to be read. The SRAM and I/O ports read operation are done by $\overline{RD}$ low (CRRWR = 0), or by E and R/$\overline{W}$ high (CRRWR = 1).

Control Signals (Cont.)

Whenever a member of the 8031 family (or any other similar microcontroller) is used, the PSD301's $\overline{PSEN}$ pin must be connected to the $\overline{PSEN}$ pin of the microcontroller.

If COMB/SEP = 0, the address spaces of the program and the data are combined. In this configuration (except for the 8031-type case mentioned above), the $\overline{PSEN}$ pin must be tied high to V_{CC}, and the EPROM, SRAM, and I/O ports are read by $\overline{RD}$ low (CRRWR = 0), or by E and R/$\overline{W}$ high (CRRWR = 1). See Figures 8 and 9.

Table 8. Signal Latch Status in All Operating Modes

Signal Name	Configuration Bits	Configuration Mode	Signal Latch Status
AD8/A8–AD15/A15	CDATA = 0, CADDRDAT = 0	8-bit data, non-multiplexed	Transparent
	CDATA = 0, CADDRDAT = 1	8-bit data, multiplexed	Transparent
	CDATA = 1, CADDRDAT = 0	16-bit data, non-multiplexed	Transparent
	CDATA = 1, CADDRDAT = 1	16-bit data, multiplexed	ALE dependent
AD0/A0–AD7/A7	CADDRDAT = 0	Non-multiplexed modes	Transparent
	CADDRDAT = 1	Multiplexed modes	ALE dependent
$\overline{BHE}$/$\overline{PSEN}$	CDATA = 0	8-bit data, $\overline{PSEN}$ is active	Transparent
	CDATA = 1, CADDRDAT = 0	16-bit data, non-multiplexed mode, $\overline{BHE}$ is active	Transparent
	CDATA = 1, CADDRDAT = 1	16-bit data, multiplexed mode, $\overline{BHE}$ is active	ALE dependent
A19 and PC2–PC0	CADDHLT = 0	A16–A19 can become logic inputs	Transparent
	CADDHLT = 1	A16–A19 can become multiplexed address lines	ALE dependent

Figure 8. Combined Address Space

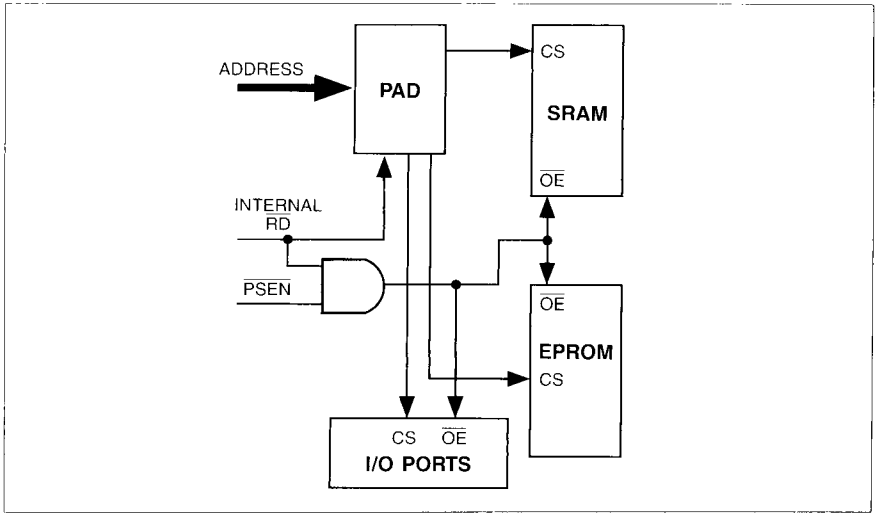
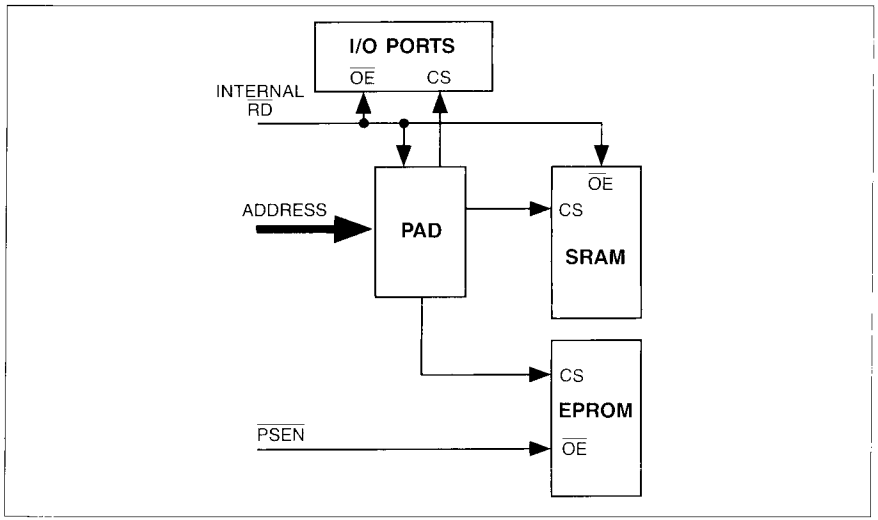


Figure 9. 8031-Type Separate Code and Data Address Spaces



In $\overline{BHE}$ mode, this pin enables accessing of the upper-half byte of the data bus. A low on this pin enables a write or read operation to be performed on the upper half of the data bus (see Table 9).

Table 9. High/Low Byte Selection Truth Table (in 16-Bit Configuration Only)

$\overline{BHE}$	A_0	Operation
0	0	Whole Word
0	1	Upper Byte From/To Odd Address (AD8–AD15)
1	0	Lower Byte From/To Even Address (AD0–AD7)
1	1	None

RESET

This is an asynchronous input pin that clears and initializes the PSD301. Reset polarity is programmable (active low or active high). Whenever the PSD301 reset input is driven active for at least 100 ns, the chip is reset. The PSD301 must be reset before it can be used. Tables 10 and 11 indicate the state of the part during and after reset.

Table 10. Signal States During and After Reset

Signal	Configuration Mode	Condition
AD0/A0–AD15/A15	All	Input
PA0–PA7 (Port A)	I/O Tracking AD0/A0–AD7/A7 Address outputs A0–A7	Input Input Low
PB0–PB7 (Port B)	I/O $\overline{CS7}$–$\overline{CS0}$ CMOS outputs $\overline{CS7}$–$\overline{CS0}$ open drain outputs	Input High Tri-stated
PC0–PC2 (Port C)	Address inputs A16–A18 $\overline{CS8}$–$\overline{CS10}$ CMOS outputs	Input High

Table 11. Internal States During and After Reset

Component	Signals	Contents
PAD	$\overline{CS0}$–$\overline{CS10}$	All = 1^{18}
	CSADIN, CSADOUT1, CSADOUT2, CSIOPORT, RS0, ES0–ES7	All = 0^{18}
Data register A	n/a	0
Direction register A	n/a	0
Data register B	n/a	0
Direction register B	n/a	0

NOTE: 18. All PAD outputs are in a non-active state.

A19/$\overline{CSI}$

When configured as $\overline{CSI}$, a high on this pin deselects, and powers down, the chip. A low on this pin puts the chip in normal operational mode. For PSD301 states during the power-down mode, see Tables 12 and 13.

Table 12. Signal States During Power-Down Mode

Signal	Configuration Mode	Condition
AD0/A0–AD15/A15	All	Input
PA0–PA7	I/O Tracking AD0/A0–AD7/A7 Address outputs A0–A7	Unchanged Input All 1's
PB0–PB7	I/O $\overline{CS7}$–$\overline{CS0}$ CMOS outputs $\overline{CS7}$–$\overline{CS0}$ open drain outputs	Unchanged All 1's Tri-stated
PC0–PC2	Address inputs A16–A18 $\overline{CS8}$–$\overline{CS10}$ CMOS outputs	Input All 1's

Table 13. Internal States During Power-Down

Component	Signals	Contents
PAD	$\overline{CS0}$–$\overline{CS10}$	All 1's (deselected)
	CSADIN, CSADOUT1, CSADOUT2, CSIOPORT, RS0, ES0–ES7	All 0's (deselected)
Data register A	n/a	All unchanged
Direction register A	n/a	
Data register B	n/a	
Direction register B	n/a	

In A19 mode, the pin is an additional input to the PAD. It can be used as a high-order address line or as a general-purpose logic input. A19 can be configured as ALE dependent or as transparent input (see Table 8). In this mode, the chip is always enabled.

Security Mode

Security Mode in the PSD301 locks the contents of the PAD A , PAD B and all the configuration bits. The EPROM, SRAM, and I/O contents can be accessed only through the PAD. The Security Mode can be set by the MAPLE or Programming software. In window packages, the mode is erasable through UV full part erasure. In the security mode, the PSD301 contents cannot be copied on a programmer.

System Applications

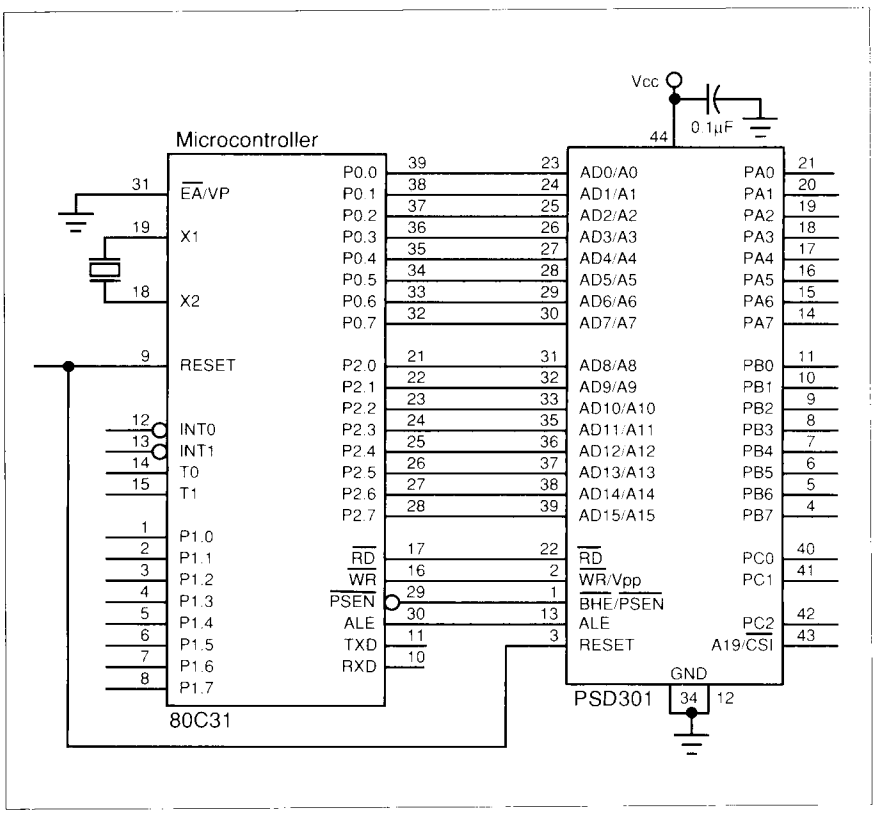
In Figure 10, the PSD301 is configured to interface with Intel's 80C31, which is a 16-bit address/8-bit data bus microcontroller. Its data bus is multiplexed with the low-order address byte. The 80C31 uses signals $\overline{RD}$ to read from data memory and $\overline{PSEN}$ to read from code memory. It uses $\overline{WR}$ to write into the data memory. It also uses active high reset and ALE signals. The rest of the configuration bits as well as the unconnected signals (not shown) are application specific and, thus, user dependent.

The configuration bits for Figure 10 are:

CRESET	1
CALE	0
CDATA	0
CADDRDAT	1
COMB/SEP	0 or 1 (both valid)
CRRWR	0

All other configuration bits may vary according to the application requirements.

Figure 10. PSD301 Interface with Intel's 80C31



System Applications (Cont.)

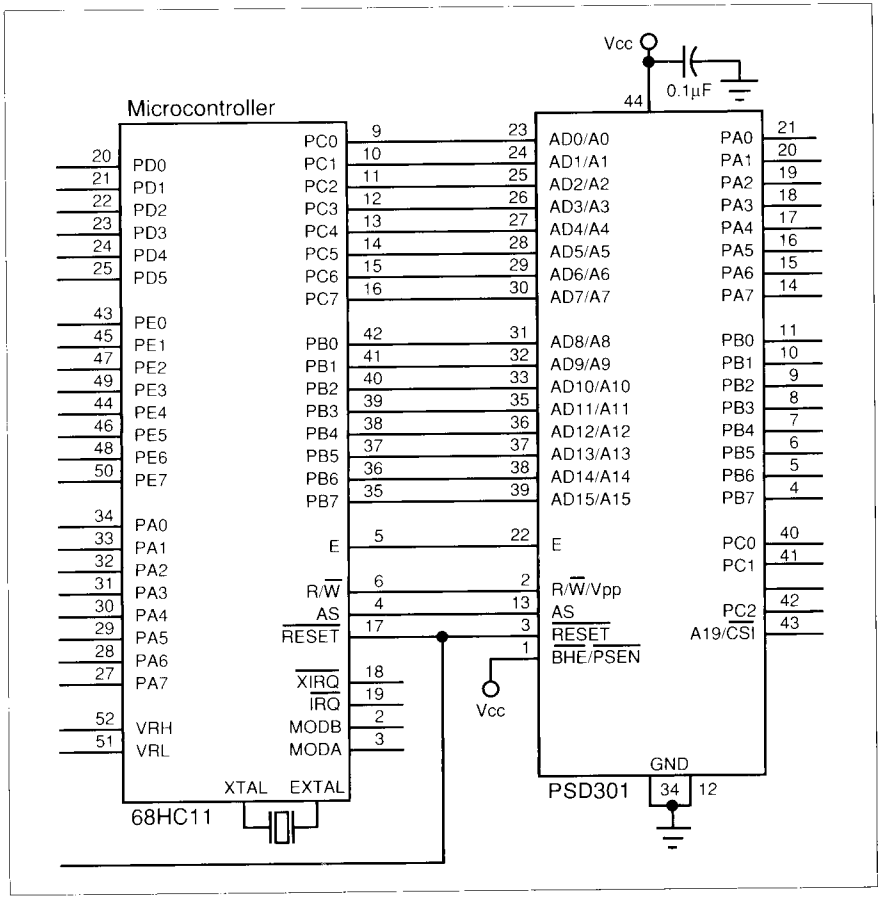
In Figure 11, the PSD301 is configured to interface with Motorola's 68HC11, which is a 16-bit address/8-bit data bus microcontroller. Its data bus is multiplexed with the low-order address byte. The 68HC11 uses E and R/$\overline{W}$ signals to derive the read and write strobes. It uses the term AS (address strobe) for the address latch pulse. RESET is an active low signal. The rest of the configuration bits as well as the unconnected signals (not shown) are application specific and, thus, user dependent.

The configuration bits for Figure 11 are:

CRESET	0
CALE	0
CDATA	0
CADDRDAT	1
COMB/SEP	0
CRRWR	1

All other configuration bits may vary according to the application requirements.

Figure 11. PSD301 Interface with Motorola's 68HC11



In Figure 12, the PSD301 is configured to work directly with Intel's 80C196KB microcontroller, which is a 16-bit address/16-bit data bus processor. Address and data lines multiplexed. In the example shown, all configuration bits are set. The PSD301 is configured to use PC0, PC1, PC2, and $\overline{CSI}$/A19 as A16, A17, A18, and A19 inputs, respectively. These signals are independent of the ALE pulse (latch-transparent). They are used as four general-purpose logic inputs that take part

System Applications (Cont.)

in the PAD equations implementation.

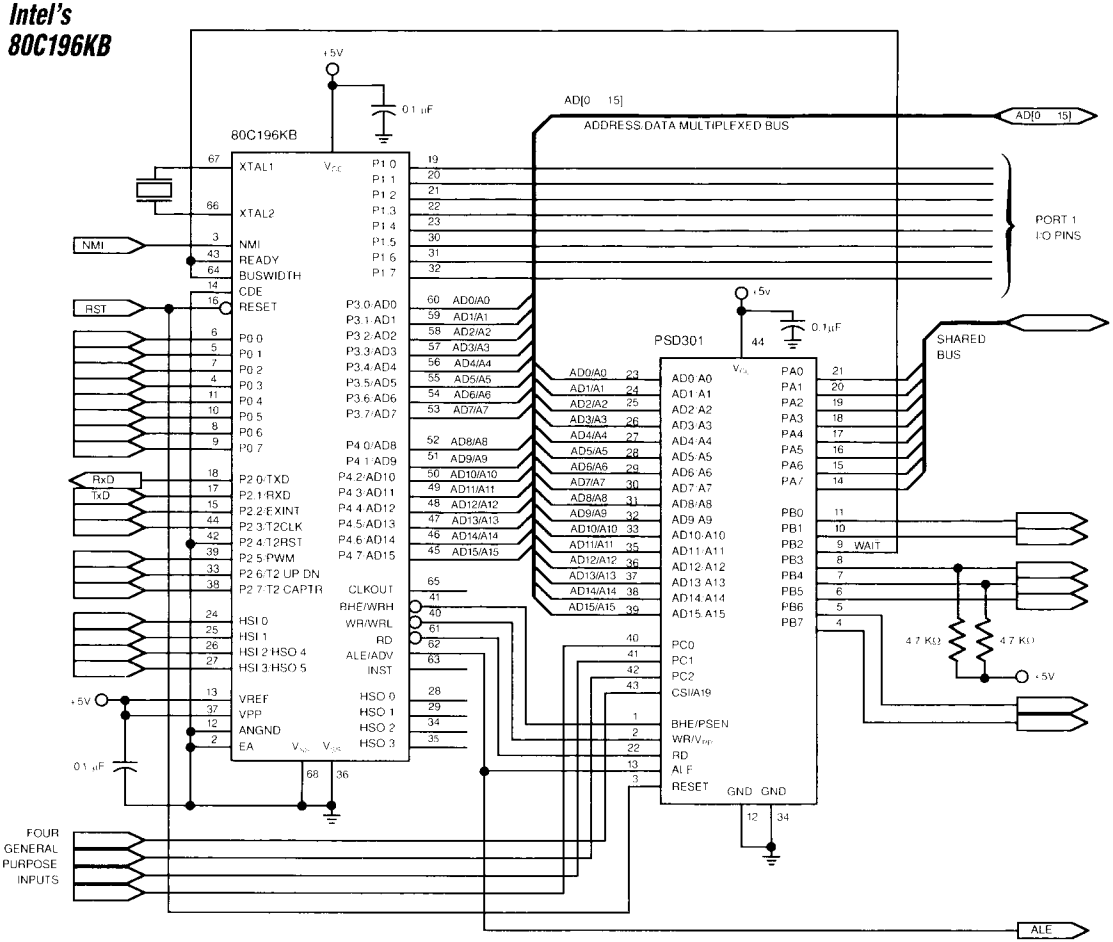
Port A is configured to work in the special track mode, in which (for certain conditions) PA0–PA7 tracks lines AD0/A0–AD7/A7. Port B is configured to generate $\overline{CS0}$–$\overline{CS7}$. In this example, PB2 serves as a $\overline{WAIT}$ signal that slows down the 80C196KB during the access of external peripherals. These 8-bit wide peripherals are connected to the shared bus of Port A. The $\overline{WAIT}$ signal also drives the buswidth input of the microcontroller, so that every external peripheral cycle becomes an 8-bit data bus cycle. PB3 and PB4 are open-drain output signals; thus, they are pulled up externally.

The configuration bits for Figure 12 are:

CRESET	0
CALE	0
CDATA	1
CADDRDAT	1
CPAF1	Don't care
CPAF2	1
CA19/$\overline{CSI}$	1
$\overline{CRRWR}$	0
$\overline{COMB/SEP}$	0
CADDHLT	0
CSECURITY	Don't care
CPCF2, CPCF1, CPCF0	0, 0, 0
CPACOD7–CPACOD0	00H
CPBF7–CPBF0	00H
CPBCOD7–CPBCOD0	18H

2

Figure 12. PSD301 Interface with Intel's 80C196KB



Absolute Maximum Ratings[19]

Symbol	Parameter	Condition	Min	Max	Unit
T_{STG}	Storage Temperature	CERDIP	– 65	+ 150	°C
		PLASTIC	– 65	+ 125	
	Voltage on any Pin	With Respect to GND	– 0.6	+ 7	V
V_{PP}	Programming Supply Voltage	With Respect to GND	– 0.6	+ 14	V
V_{CC}	Supply Voltage	With Respect to GND	– 0.6	+ 7	V
	ESD Protection			>2000	V

NOTE: 19. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at theses or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Operating Range

Range	Temperature	V_{CC}	Tolerance		
			-12	-15	-20
Commercial	0°C to + 70°C	+ 5 V	± 5%	± 10%	± 10%
Industrial	–40°C to + 85°C	+ 5 V		± 10%	± 10%
Military	–55°C to + 125°C	+ 5 V		± 10%	± 10%

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High-level Input Voltage	V_{CC} = 4.5 V to 5.5 V	2		V_{CC}	V
V_{IL}	Low-level Input Voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	V

DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	Output Low Voltage	I_{OL} = 20 µA V_{CC} = 4.5 V		0.01	0.1	V
		I_{OL} = 8 mA V_{CC} = 4.5 V		0.15	0.45	
V_{OH}	Output High Voltage	I_{OH} = –20 µA V_{CC} = 4.5 V	4.4	4.49		V
		I_{OH} = –2 mA V_{CC} = 4.5 V	2.4	3.9		
I_{SB1}	V_{CC} Standby Current (CMOS) (Notes 20 and 22)	Comm'l		50	100	µA
		Ind/Mil		75	150	
I_{SB2}	V_{CC} Standby Current (TTL) (Notes 21 and 22)	Comm'l		1.5	3	mA
		Ind/Mil		2	3.2	
I_{CC1}	Active Current (CMOS) (SRAM Not Selected) (Notes 20 and 23)	Comm'l (Note 24)		16	35	mA
		Comm'l (Note 25)		28	50	
		Ind/Mil (Note 24)		16	45	
		Ind/Mil (Note 25)		28	60	

DC Characteristics (Cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC2}	Active Current (CMOS) (SRAM Block Selected) (Notes 20 and 23)	Comm'l Note 24		47	80	mA
		Comm'l Note 25		59	95	
		Ind/Mil (Note 24)		47	100	
		Ind/Mil (Note 25)		59	115	
I_{CC3}	Active Current (TTL) (SRAM Not Selected) (Notes 21 and 23)	Comm'l (Note 24)		36	65	mA
		Comm'l (Note 25)		58	80	
		Ind/Mil (Note 24)		36	80	
		Ind/Mil (Note 25)		58	95	
I_{CC4}	Active Current (TTL) (SRAM Block Selected) (Notes 21 and 23)	Comm'l (Note 24)		67	105	mA
		Comm'l (Note 25)		79	120	
		Ind/Mil (Note 24)		67	130	
		Ind/Mil (Note 25)		79	145	
I_{LI}	Input Leakage Current	V_{IN} = 5.5 V or GND	–1	± 0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or GND	–10	± 5	10	

NOTE: 20. CMOS inputs: GND ± 0.3 V or V_{CC} ± 0.3V.
21. TTL inputs: $V_{IL} \leq 0.8$ V, $V_{IH} \geq 2.0$ V.
22. $\overline{CSI}$/A19 is high in a power-down configuration mode.
23. AC power component is 3.5 mA/MHz (power = AC + DC).
24. Ten (10) PAD product terms active. (Add 380 µA per product term, typical, or 480 µA per product term maximum.)
25. Forty-one (41) PAD product terms active.

AC Characteristics

Symbol	Parameter	-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	
T1	ALE or AS Pulse Width	30		40		50		ns
T2	Address Set-up Time	5		10		15		
T3	Address Hold Time	13		15		25		
T4	ALE or AS Trailing Edge to Leading Edge of Read	12		15		20		
T5	ALE Valid to Data Valid	140		170		220		
T6	Address Valid to Data Valid		120		150		200	
T7	$\overline{CSI}$ Active to Data Valid		150		160		200	
T8	Leading Edge of Read to Data Valid		38		55		60	
T9	Read Data Hold Time	0		0		0		
T10	Trailing Edge of Read to Data High-Z		35		40		45	
T11	Trailing Edge of ALE or AS to Leading Edge of Write	12		15		20		
T12	$\overline{RD}$, E, or $\overline{PSEN}$ Pulse Width	45		60		75		
T12A	$\overline{WR}$ Pulse Width	25		35		45		
T13	Trailing Edge of Write or Read to Leading Edge of ALE or AS	20		30		40		
T14	Address Valid to Trailing Edge of Write	120		150		200		

AC Characteristics (Cont.)

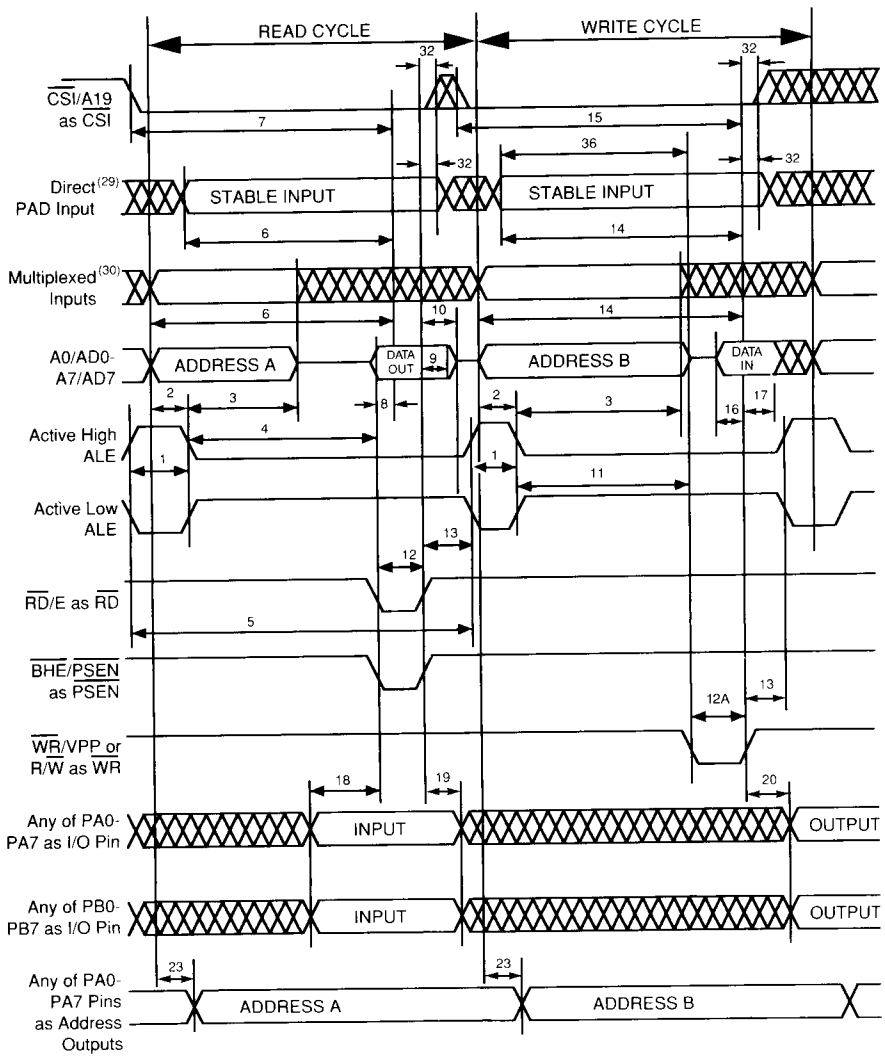
Symbol	Parameter	-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	
T15	$\overline{CSI}$ Active to Trailing Edge of Write	130		160		210		ns
T16	Write Data Set-up Time	20		30		40		
T17	Write Data Hold Time	5		10		15		
T18	Port Input Set-up Time	30		35		45		
T19	Port Input Hold Time	0		0		0		
T20	Trailing Edge of Write to Port Output Valid	40		50		60		
T21	ADi [26] or Control to $\overline{CSOi}$ [27] Valid	6	35	6	35	5	45	
T22	ADi [26] or Control to $\overline{CSOi}$ [27] Invalid	5	35	4	35	4	45	
T23	Track Mode Address Propagation Delay: • CSADOUT1 Already True or:		22		22		28	
	• CSADOUT1 Becomes True During ALE or AS		33		40		50	
T24	Track Mode Address Hold Time	15		15		27		
T25	Track Mode Read Propagation Delay		29		29		35	
T26	Track Mode Read Hold Time	11	29	10	29	10	35	
T27	Track Mode Write Cycle Data Propagation Delay		20		20		30	
T28	Track Mode Write Cycle Write to Data Propagation Delay	8	30	7	40	7	55	
T29	Hold Time of Port A Valid During Write $\overline{CSOi}$ Trailing Edge	2		4		4		
T30	$\overline{CSI}$ Active to $\overline{CSOi}$ [27] Active	9	45	9	45	8	60	
T31	$\overline{CSI}$ Inactive to $\overline{CSOi}$ [27] Inactive	9	45	9	45	8	60	
T32	Direct PAD Input [28] Hold Time	10		12		15		
T33	R/$\overline{W}$ Active to E High	20		30		40		
T34	E Low to R/$\overline{W}$ Inactive	20		30		40		
T35	AS Inactive to E High	15		20		25		

NOTES: 26. ADi = any address line.

27. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).

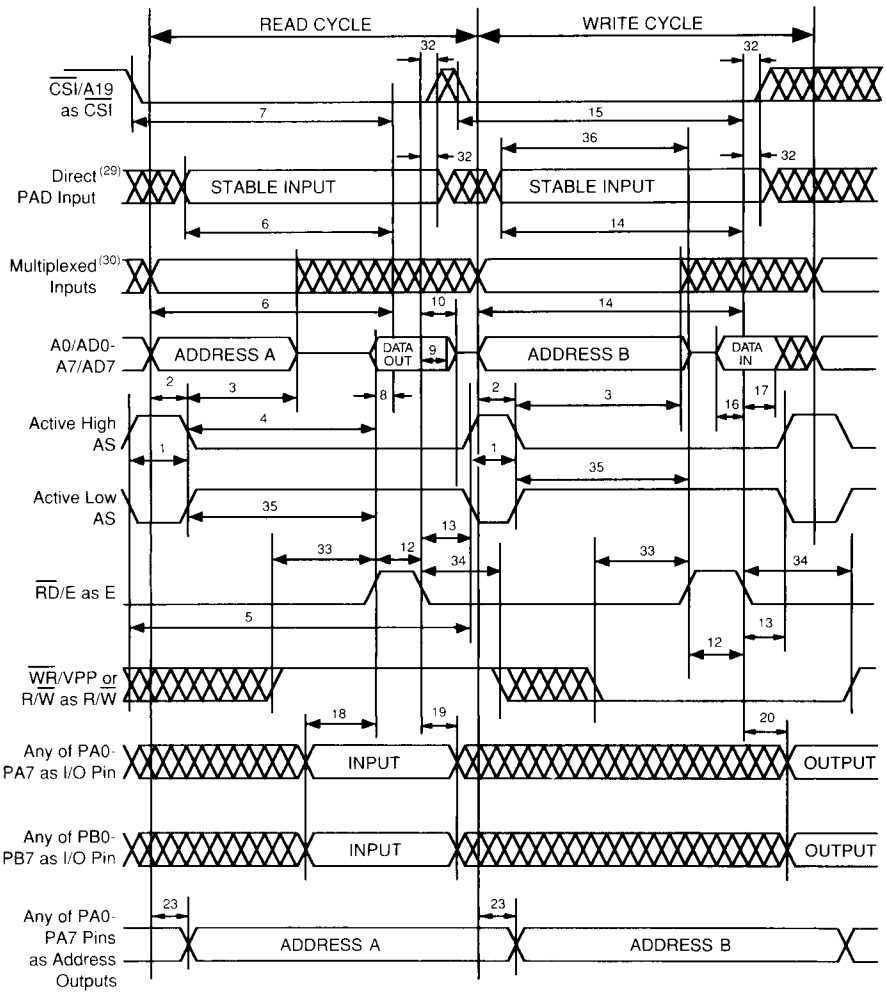
28. Direct PAD input = any of the following direct PAD input lines: CSI/A19 as transparent A19, $\overline{RD}$/E, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE (or AS).

Figure 13. Timing of 8-Bit Multiplexed Address/Data Bus, CRRWR = 0



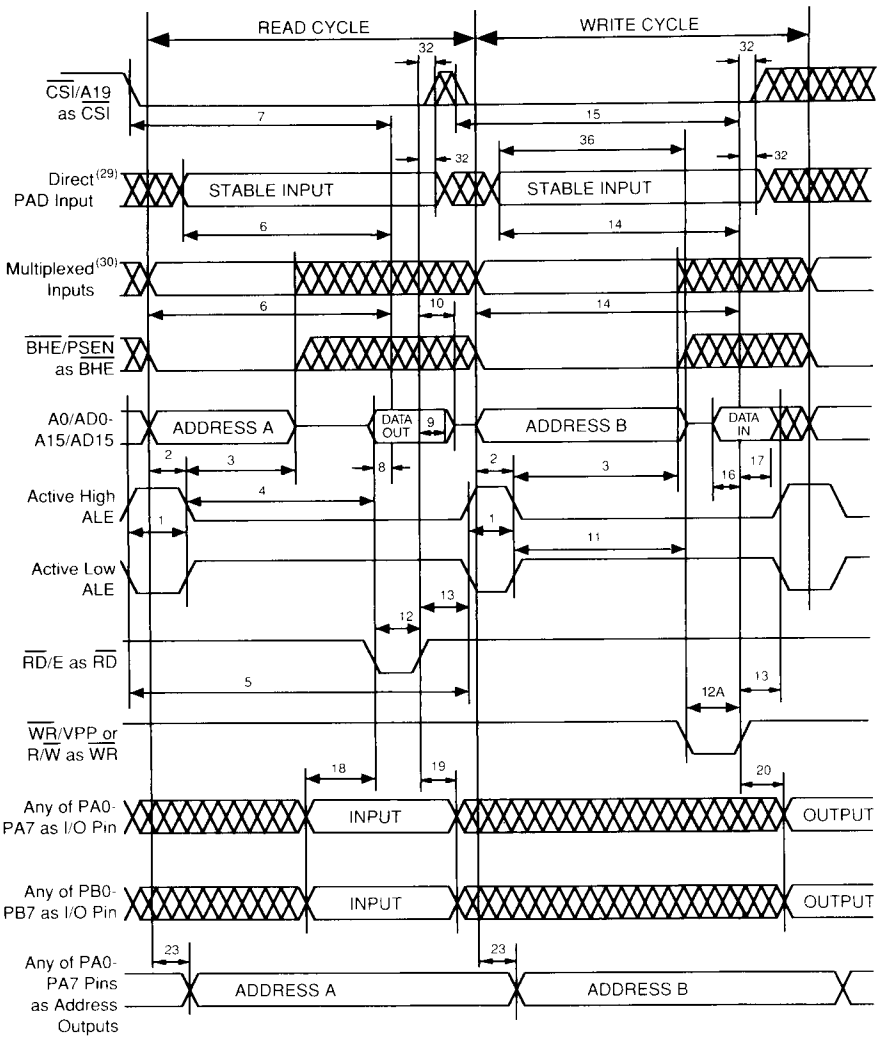
See referenced notes on page 2-36.

Figure 14. Timing of 8-Bit Multiplexed Address/Data Bus, CRRWR = 1



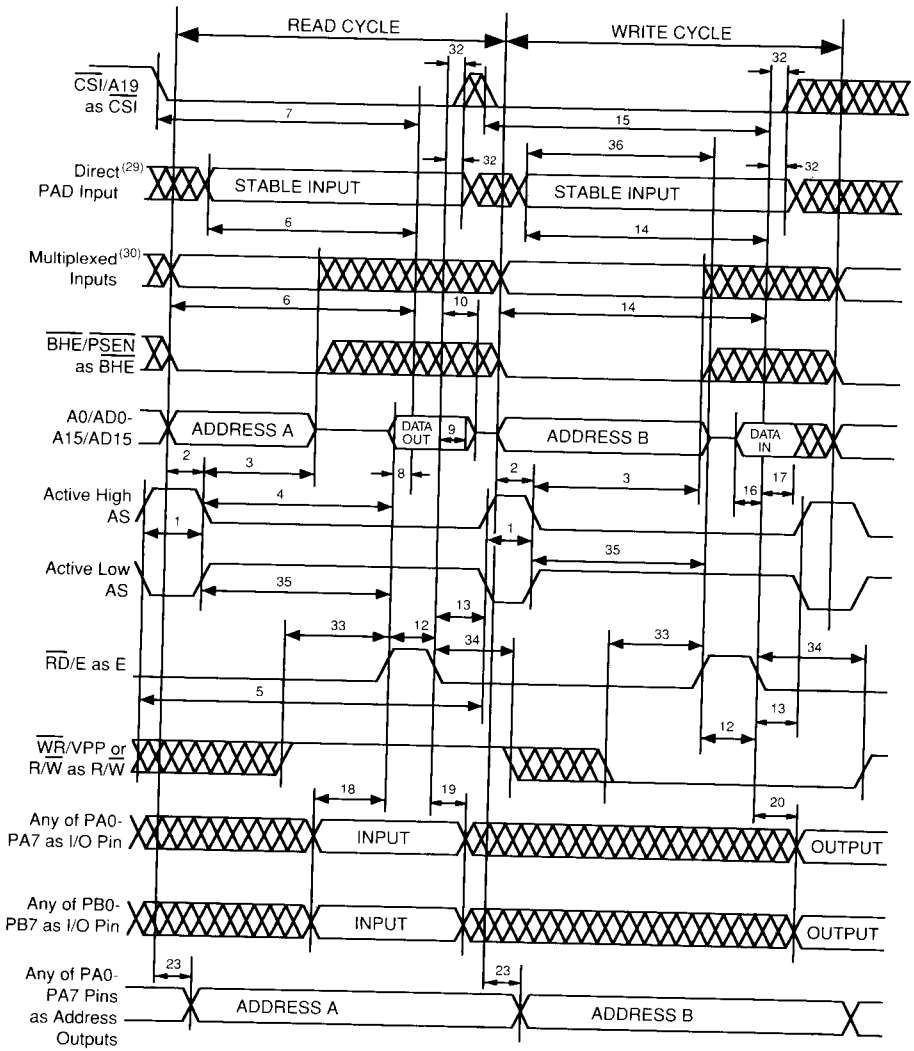
See referenced notes on page 2-36.

Figure 15. Timing of 16-Bit Multiplexed Address/Data Bus, CRRWR = 0



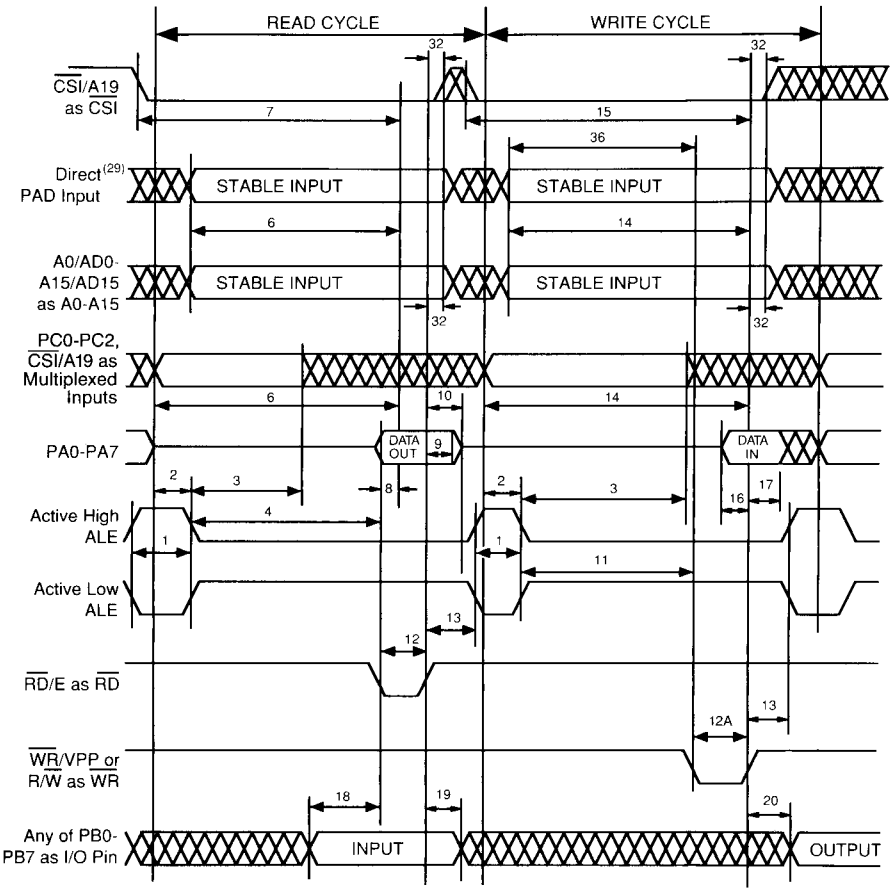
See referenced notes on page 2-36.

Figure 16. Timing of 16-Bit Multiplexed Address/Data Bus, CRRWR = 1



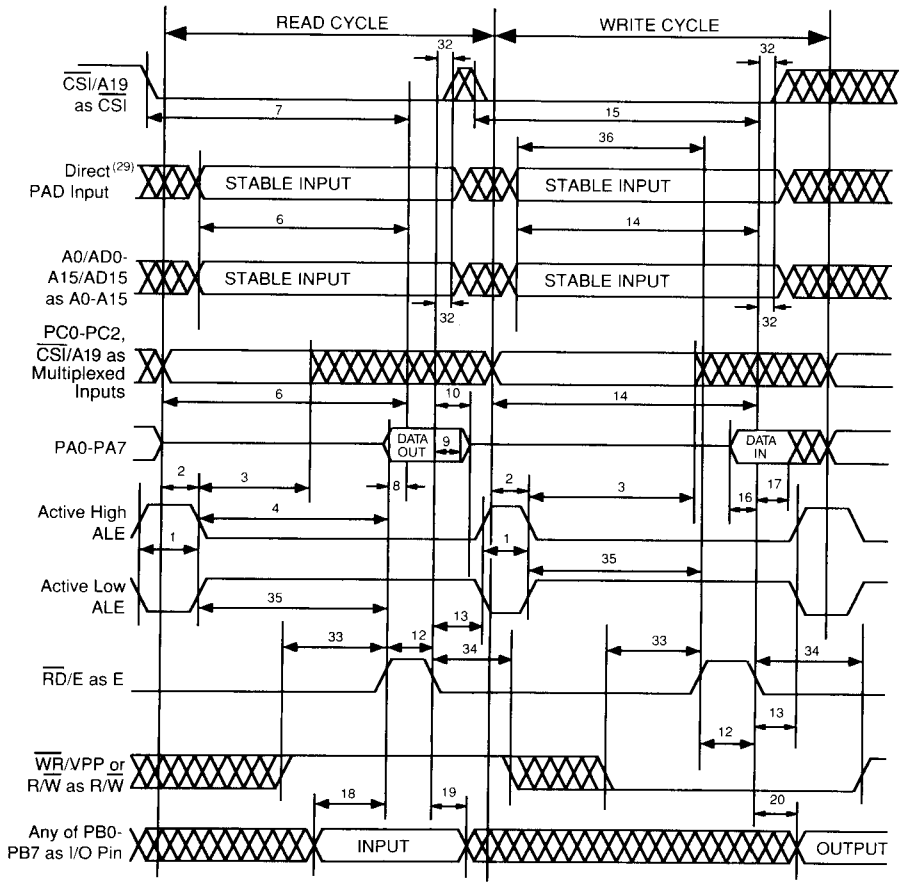
See referenced notes on page 2-36.

Figure 17. Timing of 8-Bit Data, Non-Multiplexed Address/Data Bus, CRRWR = 0



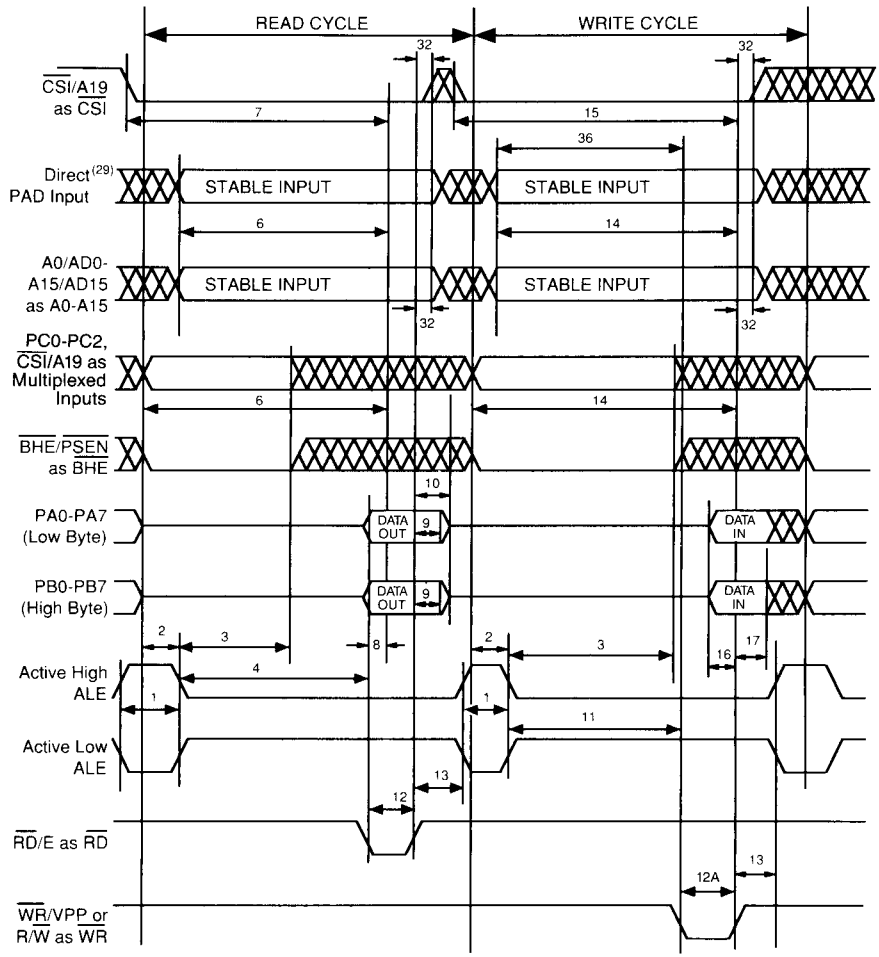
See referenced notes on page 2-36.

Figure 18. Timing of 8-Bit Data, Non-Multiplexed Address/Data Bus, CRRWR = 1



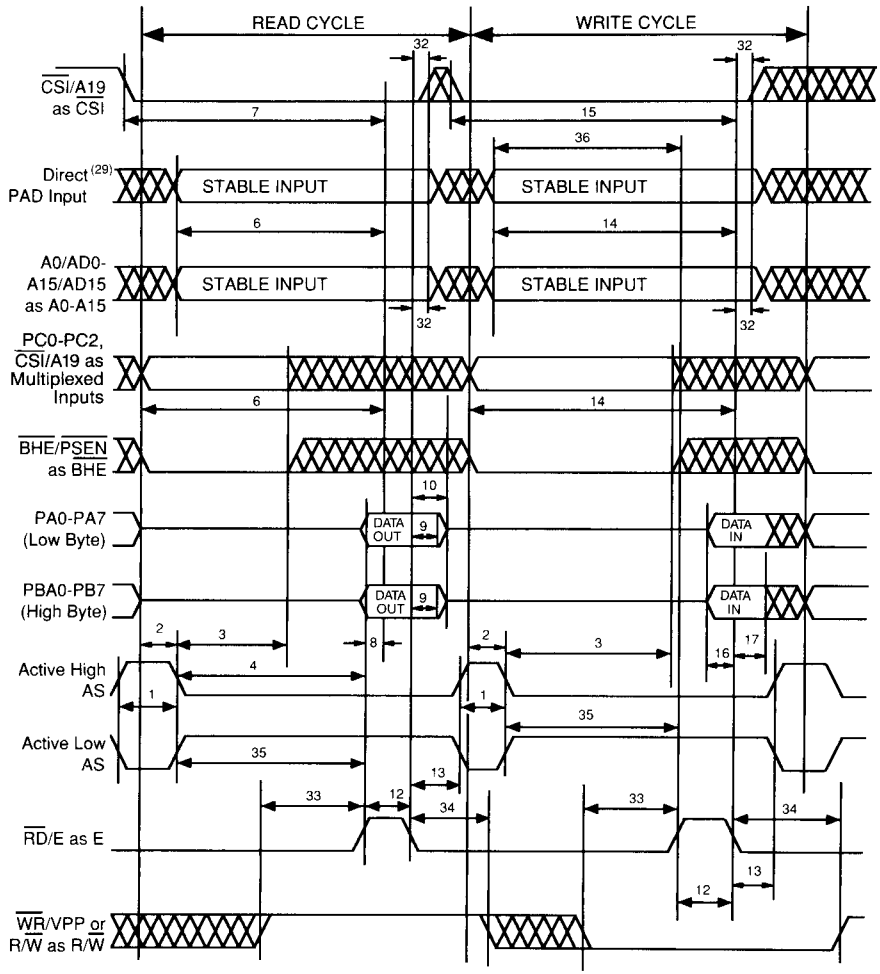
See referenced notes on page 2-36.

Figure 19. Timing of 16-Bit Non-Multiplexed Address/Data Bus, CRRWR = 0



See referenced notes on page 2-36.

Figure 20. Timing of 16-Bit Non-Multiplexed Address/Data Bus, CRRWR = 1



See referenced notes on page 2-36.

Figure 21. Chip-Select Output Timing

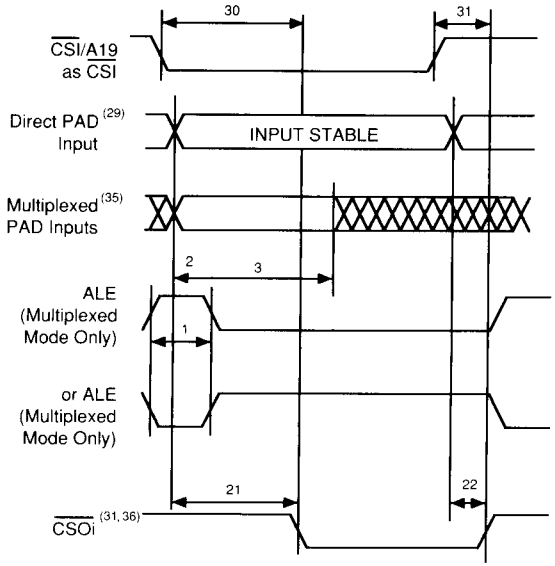
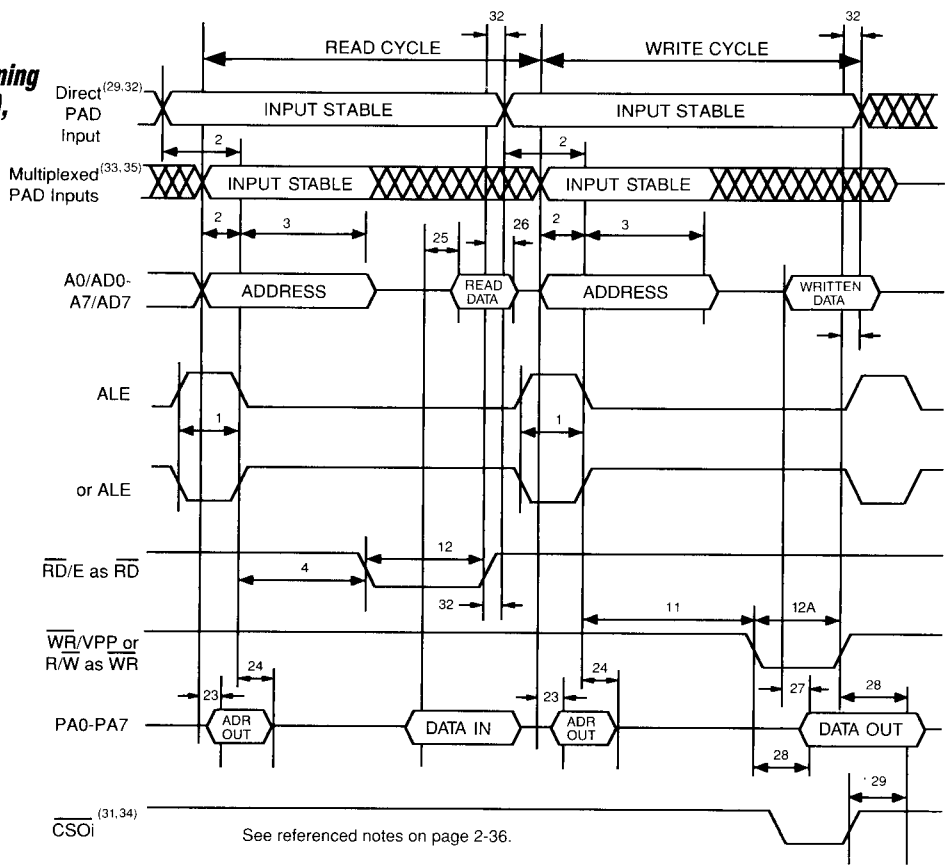
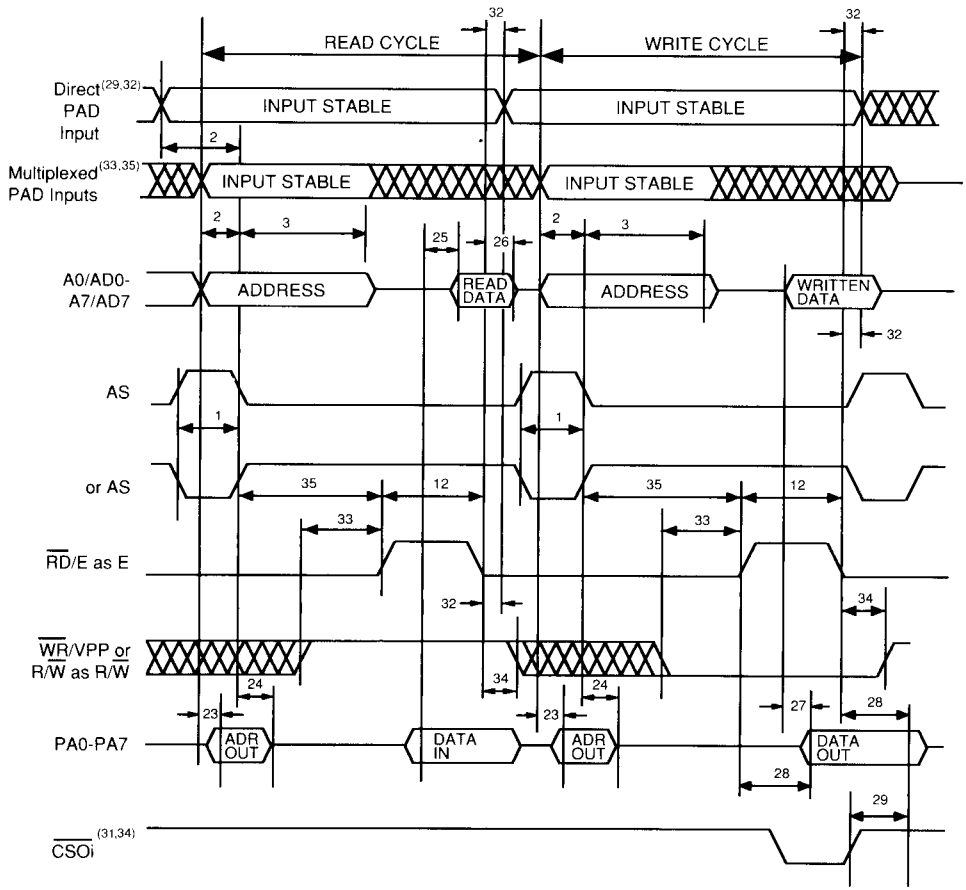


Figure 22. Port A as AD0–AD7 Timing (Track Mode), CRRWR = 0



See referenced notes on page 2-36.

Figure 23. Port A as AD0–AD7 Timing (Track Mode), CRRWR = 1



Notes for Timing Diagrams

29. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE and A11/AD11–A15/AD15 in non-multiplexed modes.
30. Multiplexed inputs: any of the following inputs that are latched by the ALE (or AS): A0/AD0–A15/AD15, $\overline{CSI}$/A19 as ALE dependent A19, ALE dependent PC0–PC2.
31. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
32. CSADOUT1, which internally enables the address transfer to Port A, should be derived only from direct PAD input signals, otherwise the address propagation delay is slowed down.
33. CSADIN and CSADOUT2, which internally enable the data-in or data-out transfers, respectively, can be derived from any combination of direct PAD inputs and multiplexed PAD inputs.
34. The write operation signals are included in the $\overline{CSOi}$ expression.
35. Multiplexed PAD inputs: any of the following PAD inputs that are latched by the ALE (or AS) in the multiplexed modes: A11/AD11–A15/AD15, $\overline{CSI}$/A19 as ALE dependent A19, ALE dependent PC0–PC2.

36 $\overline{CSOi}$ product terms can include any of the PAD input signals shown in Figure 3, except for reset and $\overline{CSI}$.

Table 14. Pin Capacitance[37]

$T_A = 25°C$, $f = 1$ MHz

Symbol	Parameter	Conditions	Typical[38]	Max	Units
C_{IN}	Capacitance (for input pins only)	$V_{IN} = 0$ V	4	6	pF
C_{OUT}	Capacitance (for input/output pins)	$V_{OUT} = 0$ V	8	12	pF
C_{VPP}	Capacitance (for $\overline{WR}/V_{PP}$ or $R/\overline{W}/V_{PP}$)	$V_{PP} = 0$ V	18	25	pF

NOTES: 37. This parameter is only sampled and is not 100% tested.
38. Typical values are for $T_A = 25°C$ and nominal supply voltages.

Figure 24. AC Testing Input/Output Waveform

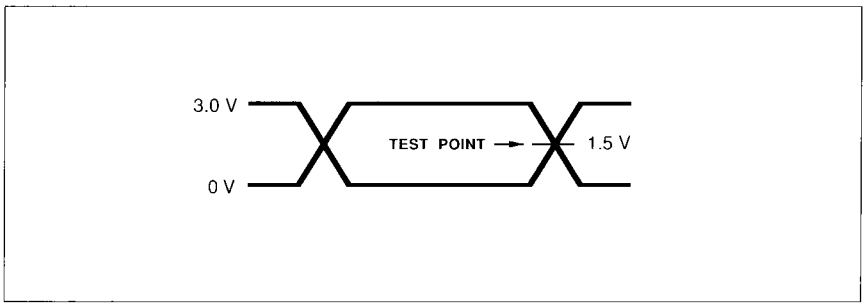
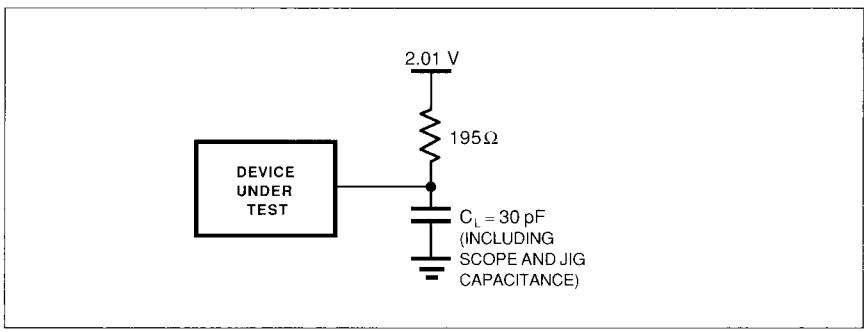


Figure 25. AC Testing Load Circuit



Erasure and Programming

To clear all locations of their programmed contents, expose the device to an ultra-violet light source. A dosage of 15 W-second/cm^2 is required. This dosage can be obtained with exposure to a wavelength of 2537 Å and intensity of 12000 µW/cm^2 for 15 to 20 minutes. The device should be about 1 inch from the source, and all filters should be removed from the UV light source prior to erasure.

The PSD301 and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although the erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight eventually erases the device. For maximum system reliability, these sources should be avoided. If used in such an environment, the package windows should be covered by an opaque substance.

Upon delivery from WSI, or after each erasure, the PSD301 device has all bits in the PAD and EPROM in the "1" or high state. The configuration bits are in the "0" or low state. The code, configuration, and PAD MAP data are loaded through the procedure of programming

Information for programming the device is available directly from WSI. Please contact your local sales representative.

PSD301 Pin Assignments

Name	44-Pin PLDCC/ CLDCC Package	44-Pin CPGA Package	52-Pin PQFP Package
$\overline{BHE}/\overline{PSEN}$	1	A_5	46
$\overline{WR}/V_{PP}$ or $R/\overline{W}$	2	A_4	47
RESET	3	B_4	48
PB7	4	A_3	49
PB6	5	B_3	50
PB5	6	A_2	51
PB4	7	B_2	2
PB3	8	B_1	3
PB2	9	C_2	4
PB1	10	C_1	5
PB0	11	D_2	6
GND	12	D_1	7
ALE or AS	13	E_1	8
PA7	14	E_2	9
PA6	15	F_1	10
PA5	16	F_2	11
PA4	17	G_1	12
PA3	18	G_2	15
PA2	19	H_2	16
PA1	20	G_3	17
PA0	21	H_3	18
$\overline{RD}/E$	22	G_4	19
AD0/A0	23	H_4	20
AD1/A1	24	H_5	21
AD2/A2	25	G_5	22
AD3/A3	26	H_6	23
AD4/A4	27	G_6	24
AD5/A5	28	H_7	25
AD6/A6	29	G_7	28
AD7/A7	30	G_8	29
AD8/A8	31	F_7	30
AD9/A9	32	F_8	31
AD10/A10	33	E_7	32
GND	34	E_8	33
AD11/A11	35	D_8	34
AD12/A12	36	D_7	35
AD13/A13	37	C_8	36
AD14/A14	38	C_7	37
AD15/A15	39	B_8	38
PC0	40	B_7	41
PC1	41	A_7	42
PC2	42	B_6	43
A19/$\overline{CSI}$	43	A_6	44
V_{CC}	44	B_5	45

Package Information

Figure 26. Drawing L4 — 44 Pin Ceramic Leaded Chip Carrier (CLDCC) with Window (Package Type L)

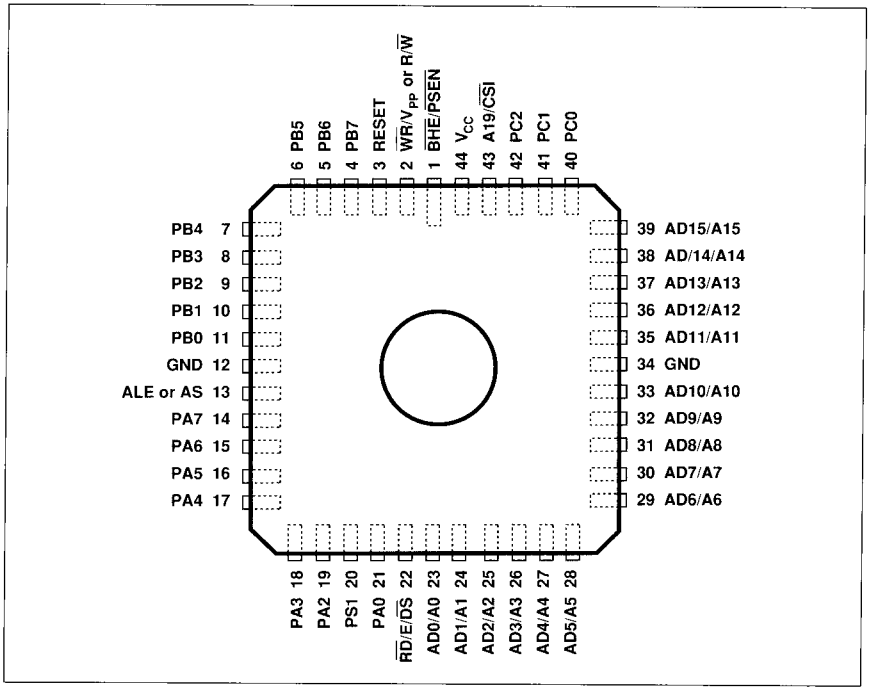


Figure 27. Drawing J2 — 44-Pin Plastic Leaded Chip Carrier (PLDCC) (Package Type J)

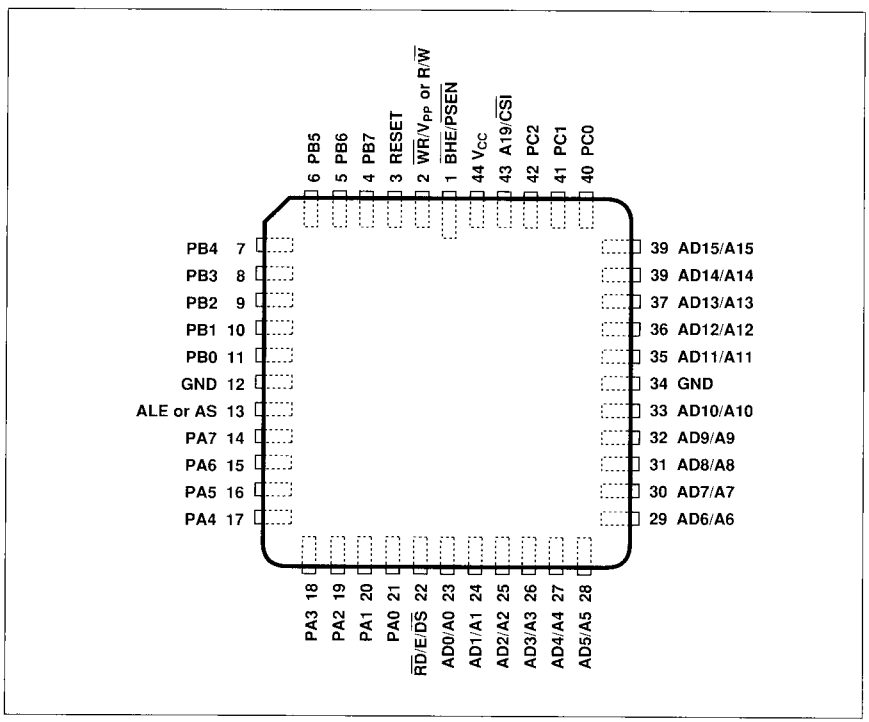


Figure 28. Drawing Q2 — 52-Pin PQFP (Package Type Q)

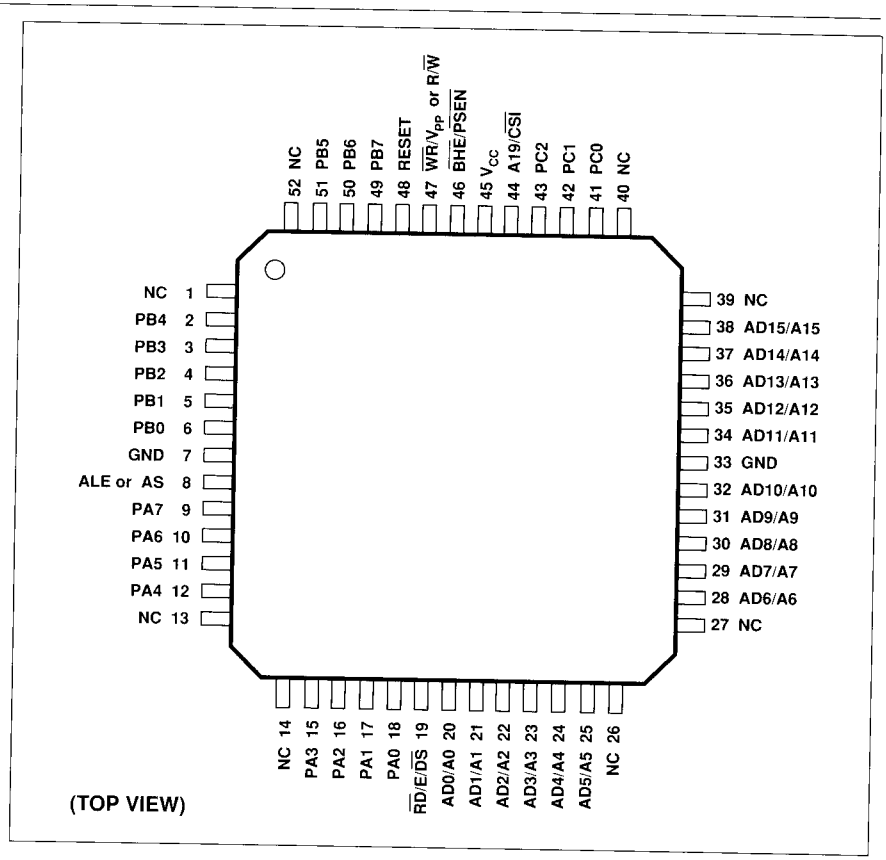
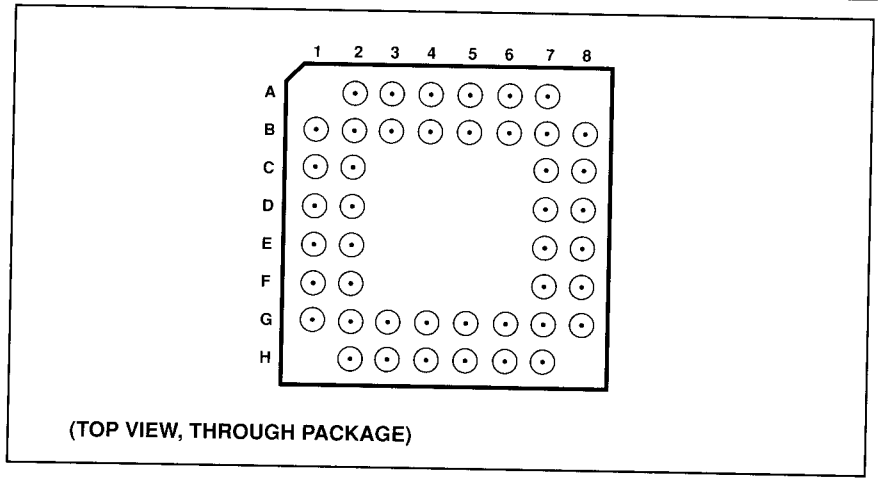


Figure 29: Drawing X2 — 44-Pin CPGA (Package Type X)



Ordering Information

Part Number	Spd. (ns)	Package Type	Package Drawing	Operating Temperature Range	WSI Manufacturing Procedure
PSD301-12J	120	44-pin PLDCC	J2	Commercial	Standard
PSD301-12L	120	44-pin CLDCC	L4	Commercial	Standard
PSD301-12Q	120	52-pin PQFP	Q2	Commercial	Standard
PSD301-15J	150	44-pin PLDCC	J2	Commercial	Standard
PSD301-15JI	150	44-pin PLDCC	J2	Industrial	Standard
PSD301-15L	150	44-pin CLDCC	L4	Commercial	Standard
PSD301-15LI	150	44-pin CLDCC	L4	Industrial	Standard
PSD301-15Q	150	52-pin PQFP	Q2	Commercial	Standard
PSD301-15X	150	44-pin CPGA	X2	Commercial	Standard
PSD301-20J	200	44-pin PLDCC	J2	Commercial	Standard
PSD301-20JI	200	44-pin PLDCC	J2	Industrial	Standard
PSD301-20L	200	44-pin CLDCC	L4	Commercial	Standard
PSD301-20LI	200	44-pin CLDCC	L4	Industrial	Standard
PSD301-20LM	200	44-pin CLDCC	L4	Military	Standard
PSD301-20LMB	200	44-pin CLDCC	L4	Military	MIL-STD-883C
PSD301-20Q	200	52-pin PQFP	Q2	Commercial	Standard
PSD301-20X	200	44-pin CPGA	X2	Commercial	Standard
PSD301-20XI	200	44-pin CPGA	X2	Industrial	Standard
PSD301-20XM	200	44-pin CPGA	X2	Military	Standard
PSD301-20XMB	200	44-pin CPGA	X2	Military	MIL-STD-883C

System Development Tools

The PSD301 features a complete set of System Development Tools. These tools provide an integrated, easy-to-use software and hardware environment to support PSD301 device development. To run these tools requires an IBM-XT, -AT, or compatible computer, MS-DOS 3.1 or higher, 640K byte RAM, and a hard disk.

Hardware

The PSD301 System Programming Hardware consists of:

- ❑ WS6000 MagicPro Memory and PSD Programmer
- ❑ WS6015 44-pin CPGA Package Adaptor
- ❑ WS6020 52-pin PQFP Package Adaptor
- ❑ WS6021 44-pin LCC Package Adaptor (for CLDCC and PLDCC packages)

The MagicPro Programmer is the common hardware platform for programming all WSI programmable products. It consists of an IBM-PC plug-in programmer board and a remote socket adaptor.

Software

The PSD301 System Development Software consists of:

- ❑ WISPER, WSI's Software Environment
- ❑ MAPLE, the PSD301 Location Editor Software
- ❑ WS6021 44-pin LCC Package Adaptor (for CLDCC and PLDCC Packages)

The configuration of the PSD301 device is entered using MAPLE software. MAPPRO software uses the MagicPro programmer and the socket adaptor to configure the PSD301 device, which then can be used. The development cycle is depicted in Figure 30.

Support

WSI provides a complete set of quality support services to registered System Development Tools owners, including:

- ❑ 12-month software updates
- ❑ Design assistance from WSI field application engineers and application group experts
- ❑ 24-hour electronic bulletin board for design assistance via dial-up modem.

Training

WSI provides in-depth, hands-on workshops for the PSD301 device and System Development Tools. Workshop participants learn how to program high-performance, user-configurable mappable memory subsystems. Workshops are held at the WSI facility in Fremont, California.

Ordering Information – System Development Tools

PSD-GOLD

- ❑ WISPER Software
- ❑ MAPLE Software
- ❑ User's Manual
- ❑ WSI Support
- ❑ WS6000 MagicPro™ Programmer
- ❑ One Package Adaptor and Two PSD301 Product Samples

PSD-SILVER

- ❑ WISPER Software
- ❑ MAPLE software
- ❑ User's Manual
- ❑ WSI Support

WS6000

- ❑ MagicPro Programmer
- ❑ IBM-PC© Plug-in Adaptor Card
- ❑ Remote Socket Adaptor

WS6015

- ❑ 44-pin CPGA Package Adaptor; Used with WS6000 MagicPro Programmer

WS6020

- ❑ 52-pin PQFP Package Adaptor; Used with the WS6000 MagicPro Programmer

WS6021

- ❑ 44-Pin Package Adaptor for CLDCC and PLDCC Packages; Used with the WS6000 MagicPro Programmer

WSI Support

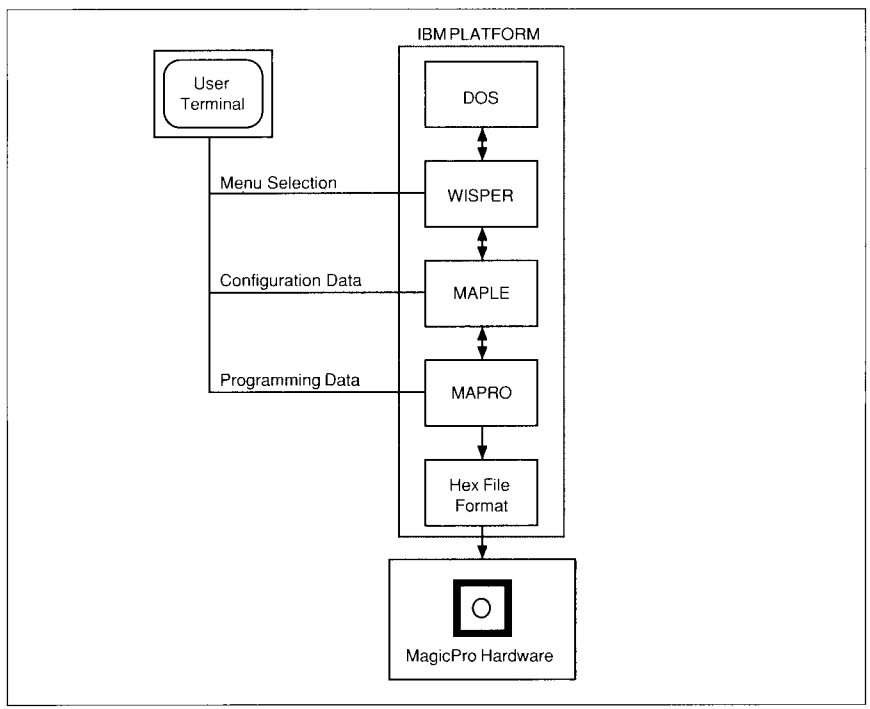
Support services include:

- ❑ 12-month Software Update Service
- ❑ Hotline to WSI Application Experts
- ❑ 24-hour access to WSI Electronic Bulletin Board

WSI Training

- ❑ Workshops at WSI, Fremont, CA
- ❑ For details and scheduling, call PSD Marketing (510) 656-5400.

Figure 30. PSD301 Development Cycle



Programmable Peripheral

PSD311

Programmable Microcontroller Peripheral with Memory

Key Features

- ❑ Single Chip Programmable Peripheral for Microcontroller-based Applications
- ❑ 19 Individually Configurable I/O pins that can be used as
  - — Microcontroller I/O port expansion
  - — Programmable Address Decoder (PAD) I/O
  - — Latched address output
  - — Open drain or CMOS
- ❑ Two Programmable Arrays (PAD A & PAD B)
  - — Total of 40 Product Terms and up to 16 Inputs and 24 Outputs
  - — Direct Address Decoding up to 1 Meg address space
  - — Logic replacement
- ❑ "No Glue" Microcontroller Chip-Set
  - — Built-in address latches for multiplexed address/data bus
  - — Non-multiplexed address/data bus mode
  - — 8 bit data bus width
  - — ALE and Reset polarity programmable
  - — Selectable modes for read and write control bus as $\overline{RD}/\overline{WR}$, $R/\overline{W}/E$
  - — PSEN/ pin for 8051 users
- ❑ 256 Kbits of UV EPROM
  - — Organized as 32K x 8
  - — Divides into 8 equal mappable blocks for optimized mapping
  - — Block resolution is 4K x 8
  - — 120 ns EPROM access time, including input latches and PAD address decoding.
- ❑ 16 Kbit Static RAM
  - — Organized as 2K x 8
  - — 120 ns SRAM access time, including input latches and PAD address decoding
- ❑ Address/Data Track Mode
  - — Enables easy Interface to Shared Resources (Mail Box SRAM) with other Microcontrollers or a Host Processor
- ❑ Built-In Security
  - — Locks the PSD311 Configuration and PAD Decoding
- ❑ Available in a Variety of Packaging
  - — 44 Pin PLDCC and CLDCC
  - — 52 Pin PQFP
  - — 44 Pin CPGA
- ❑ Simple Menu-Driven Software: Configure the PSD311 on an IBM PC

Partial Listing of Microcontrollers Supported

- ❑ **Motorola family:** M6805, M68HC11, M68HC16, M68000/10/20, M60008, M683XX
- ❑ **Intel family**: 8031/8051, 8098, 80188, 80198
- ❑ **Signetics:** SC80C451
- ❑ **Zilog:** Z8, Z80, Z180

Applications

- ❑ Computers (Workstations and PCs)
  - — Fixed Disk Control, Modem, Imaging, Laser Printer Control
- ❑ Telecommunications
  - — Modem, Cellular Phone, Digital PBX, Digital Speech, FAX, Digital Signal Processing
- ❑ Industrial
  - — Robotics, Power Line Access, Power Line Motor
- ❑ Medical Instrumentation
  - — Hearing Aids, Monitoring Equipment, Diagnostic Tools
- ❑ Military
  - — Missile Guidance, Radar, Sonar, Secure Communications, RF Modems

Introduction

The PSD311 is the latest member in the rapidly growing WSI family of PSD devices. The PSD311 is ideal for microcontroller-based applications, where fast time-to-market, small form factor, and low power consumption are essential. When combined in a system, virtually any microcontroller (68HC11, 8051 etc.) and the PSD311 work together to create a very powerful chip-set solution. This implementation provides all the required control and peripheral elements of a microcontroller-based system peripheral with no external discrete "glue" logic required.

The solution comes complete with simple system software development tools for integrating the PSD311 with the microcontroller. Hosted on the IBM PC platforms or compatibles, the easy to use software enables the designer complete freedom in designing the system.

Product Description

The PSD311 integrates high performance user-configurable blocks of EPROM, SRAM, and programmable logic technology to provide a single chip microcontroller interface. The major functional blocks include two programmable logic arrays, PAD A and PAD B, 256K bits of EPROM, 16K bits of SRAM, input latches, and output ports. The PSD311 is ideal for applications requiring high performance, low power, and very small form factors. These include fixed disk control, modem, cellular telephone, instrumentation, computer peripherals, military and similar applications.

The PSD311 offers a unique single-chip solution for microcontrollers that need:

- ❑ I/O reconstruction (microcontrollers lose at least two I/O ports when accessing external resources).
- ❑ More EPROM and SRAM than the microcontroller's internal memory.
- ❑ Chip-select, control, or latched address lines that are otherwise implemented discretely.
- ❑ An interface to shared external resources.

WSI's PSD311 (shown in Figure 1) can efficiently interface with, and enhance, any microcontroller system. This is the first solution that provides microcontrollers with port expansion, latched addresses, page logic, two programmable logic arrays PAD A and PAD B, an interface to shared resources, 256K bit EPROM, and 16K bit SRAM on a single chip. The PSD311 does not require any glue logic for interfacing to any 8-bit microcontroller.

The 8051 microcontroller family can take full advantage of the PSD311's separate program and data address spaces. Users of the 68HCXX family of microcontrollers can change the functionality of the control signals and directly connect the R/W and E. Address and data buses can be configured to be separate or multiplexed, whichever is required by the host processor.

Product Discription (Cont.)

The flexibility of the PSD311 I/O ports permits interfacing to shared resources. The arbitration can be controlled internally by PAD A outputs. The user can assign the following functions to these ports: standard I/O pins, chip-select outputs from the PAD A and PAD B, or latched address or multiplexed low-order address/data byte. This enables users to design add-on systems such as disk drives, modems, etc., that easily interface to the host bus (e.g., IBM PC, SCSI).

The PSD311 on-chip programmable address decoder (PAD A) enables the user to map the I/O ports, eight segments of EPROM (4K x 8 each) and SRAM (2K x 8) anywhere in the address space of the microcontroller. PAD B can implement up to 4 sum-of-product expressions based on address inputs and control signals.

Figure 1. PSD311 Architecture

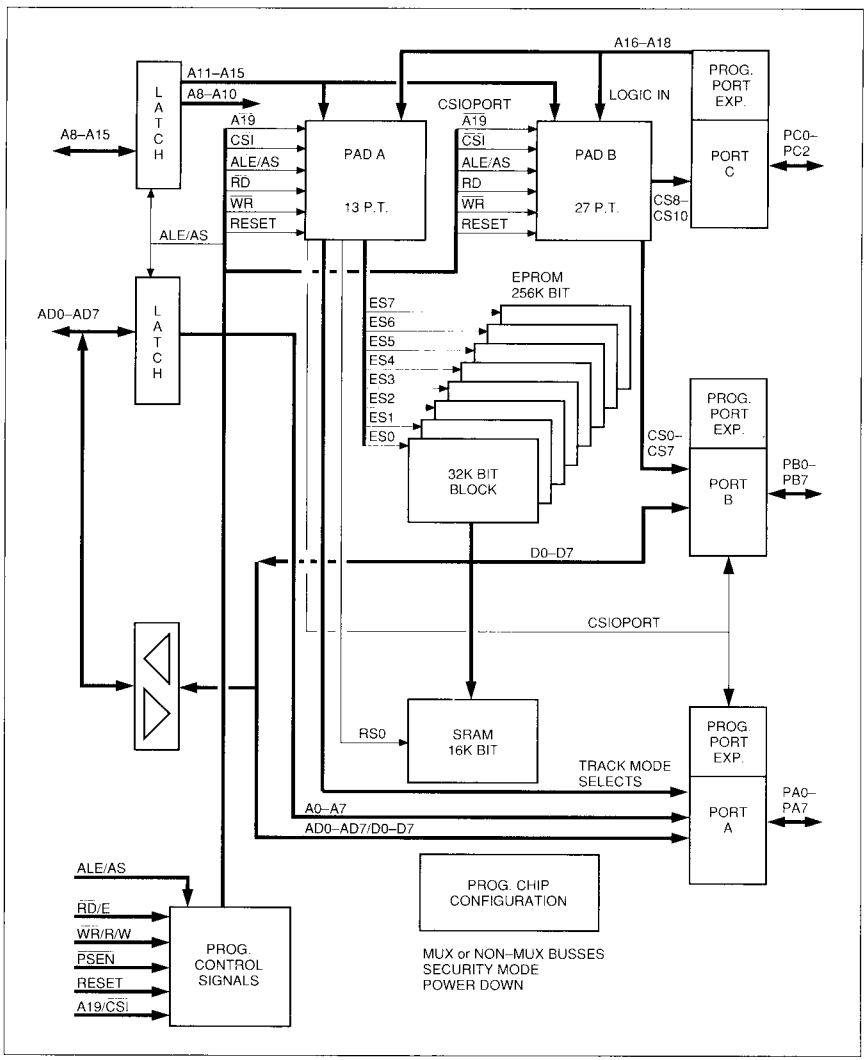


Table 1. PSD311 Pin Descriptions

Name	Type	Description
$\overline{PSEN}$	I	The $\overline{PSEN}$ is the active low EPROM read pulse. The SRAM and I/O ports read signal is generated according to the description of the $\overline{WR}/V_{PP}$ or R/$\overline{W}$, and $\overline{RD}$/E pins. If the host processor is a member of the 8031 family, $\overline{PSEN}$ must be connected to the corresponding host pin. In other 8-bit host processors that do not have a special EPROM-only read strobe, $\overline{PSEN}$ should be tied to V_{CC}. In this case, $\overline{RD}$ or E and R/$\overline{W}$ provide the read strobe for the SRAM, I/O ports, and EPROM.
$\overline{WR}/V_{PP}$ or R/$\overline{W}$/V_{PP}	I	In the operating mode, this pin's function is $\overline{WR}$ (CRRWR = 0) or R/$\overline{W}$ (CRRWR = 1). When configured as $\overline{WR}$, a write operation is executed during an active low pulse. When configured as R/$\overline{W}$, with R/$\overline{W}$ = 1 and E = 1, a read operation is executed; if R/$\overline{W}$ = 0 and E = 1, a write operation is executed. In programming mode, this pin must be tied to V_{PP} voltage.
$\overline{RD}$/E	I	When configured as $\overline{RD}$ (CRRWR = 0), this pin provides an active low $\overline{RD}$ strobe. When configured as E (CRRWR = 1), this pin becomes an active high pulse, which, together with R/$\overline{W}$ defines the cycle type. Then, if R/$\overline{W}$ = 1 and E = 1, a read operation is executed. If R/$\overline{W}$ = 0 and E = 1, a write operation is executed.
$\overline{CSI}$/A19		This pin has two configurations. When it is $\overline{CSI}$ (CA19/$\overline{CSI}$ = 0) and the pin is asserted high, the device is deselected and powered down. (See Tables 10 and 11 for the chip state during power-down mode.) If the pin is asserted low, the chip is in normal operational mode. When it is configured as A19, (CA19/$\overline{CSI}$ = 1), this pin can be used as an additional input to the PAD. CADLOG3 = 1 defines the pin as an address; CADLOG3 = 0 defines it as a logic input. If it is an address, A19 can be latched with ALE (CADDHLT = 1) or be a transparent logic input (CADDHLT = 0). In this mode, there is no power-down capability.
RESET	I	This user-programmable pin can be configured to reset on high level (CRESET = 1) or on low level (CRESET = 0). It should remain active for at least 100 ns. See Tables 8 and 9 for the chip state after reset.
ALE or AS	I	In the multiplexed modes, the ALE pin functions as an Address Latch Enable or as an Address strobe and can be configured as an active high or active low signal. The ALE or AS trailing edge latches lines AD7/A7–AD0/A0, A16–A19, and $\overline{BHE}$, depending on the PSD311 configuration. See Table 7. In the non-multiplexed modes, it can be used as a general-purpose logic input to the PAD.

Legend: The I/O column abbreviations are: I = input; I/O = input/output; P = power.

NOTE: 1. All the configuration bits mentioned in Table 1 appear in parentheses and are explained in the Configuration Register section.

Table 1. PSD311 Pin Descriptions (Cont.)

Name	Type	Description
PA7 PA6 PA5 PA4 PA3 PA2 PA1 PA0	I/O	PA7–PA0 is an 8-bit port that can be configured to track AD7/A7–AD0/A0 from the input (CPAF2 = 1). Otherwise (CPAF2 = 0), each bit can be configured separately as an I/O or lower-order latched address line. When configured as an I/O (CPAF1 = 0), the direction of the pin is defined by its direction bit, which resides in the direction register. If a pin is an I/O output, its data bit (which resides in the data register) comes out. When it is configured as a low-order address line (CPAF1 = 1), A7–A0 can be made the corresponding output through this port (e.g., PA6 can be configured to be the A6 address line). Each port bit can be a CMOS output (CPACOD = 0) or an open drain output (CPACOD = 1). When the chip is in non-multiplexed mode (CADDRDAT = 0), the port becomes the data bus lines (D0–D7). See Figure 4.
PB7 PB6 PB5 PB4 PB3 PB2 PB0	I/O	PB7–PB0 is an 8-bit port for which each bit can be configured as an I/O (CPBF = 1) or chip-select output (CPBF = 0). Each port bit can be a CMOS output (CPBCOD = 0) or an open drain output (CPBCOD = 1). When configured as an I/O, the direction of the pin is defined by its direction bit, which resides in the direction register. If a pin is an I/O output, its data (which resides in the data register) comes out. When configured as a chip-select output, $\overline{CS0}$–$\overline{CS3}$ are a function of up to four product terms of the inputs to the PAD B; $\overline{CS4}$,–$\overline{CS7}$ then are each a function of up to two product terms. See Figure 6.
PC0 PC1 PC2	I/O	This is a 3-bit port for which each bit is configurable as a PAD input or output. When configured as an input (CPCF = 0), the bits can be latched with ALE (CADDHLT = 1) or be transparent inputs to the PAD (CADDHLT = 0). When a pin is configured as an output (CPCF = 1), it is a function of one product term of all PAD inputs. See Figure 7.
AD0/A0 AD1/A1 AD2/A2 AD3/A3 AD4/A4 AD5/A5 AD6/A6 AD7/A7	I/O	In multiplexed mode, these pins are the multiplexed low-order address/data byte. After ALE latches the addresses, these pins input or output data, depending on the settings of the $\overline{RD}$/E, $\overline{WR}$/V_{PP} or R/$\overline{W}$, and $\overline{PSEN}$ pins. In non-multiplexed mode, these pins are the low-order address input.
A8 A9 A10 A11 A12 A13 A14 A15	I/O	These pins are the high-order address input.
GND	P	V_{SS} (ground) pin.
V_{CC}	P	Supply voltage input.

Operating Modes

The PSD311's two operating modes allow it to interface directly to 8-bit microcontrollers with multiplexed and non-multiplexed address/data buses. These operating modes are described below.

Multiplexed 8-bit Address/Data Bus

This mode is used to interface to microcontrollers with an 8-bit data bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is bidirectional and permits the latching of the address when the ALE signal is active. On the same pins, the data is read from or written to the device; this depends on the state of the $\overline{RD}$/E, $\overline{PSEN}$ and $\overline{WR}/V_{PP}$ or R/$\overline{W}$ pins. The high-order address bus (A8–A15) contains the high-order address bus byte. Ports A and B can be configured as in Table 2.

Non-Multiplexed Address/Data, 8-bit Data Bus

This mode is used to interface to a microcontroller with an 8-bit non-multiplexed bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is the low-order address input bus. The high-order address/data bus (A8–A15) is the high-order address bus byte. Port A is the low-order data bus. Port B can be configured as shown in Table 2.

Table 2 summarizes the effect of the different operating modes on ports A, B, and the address/data pins. The configuration of Port C is independent of the four operating modes.

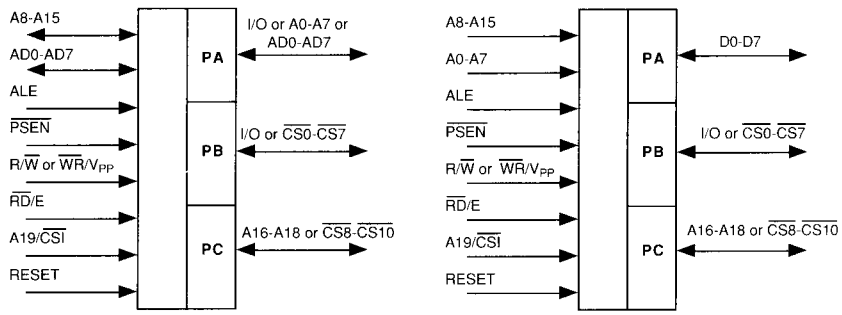
Programmable Address Decoder (PAD)

The PSD311 consists of two programmable arrays referred to as PAD A and PAD B (Figure 3). PAD A is used to generate chip select signals derived from the input address to the internal EPROM blocks, SRAM, I/O ports, and Track Mode signals. All its I/O functions are listed in Table 3 and shown in Figure 3. PAD B outputs to Ports B and C for off-chip usage.

PAD B can also be used to extend the decoding to select external devices or as a random logic replacement. The input bus to both PAD A and PAD B is the same. Using WSI's MAPLE software, each programmable bit in the PAD's array can have one of three logic states of 0, 1, and don't care (X). In a user's logic design, both PADs can share the same inputs using the X for input signals that are not supposed to affect other functions. The PADs use reprogrammable CMOS EPROM technology and can be programmed and erased by the user.

Figure 2. PSD311 Port Configurations

Figure 2 shows the PSDS311's I/O port configurations.



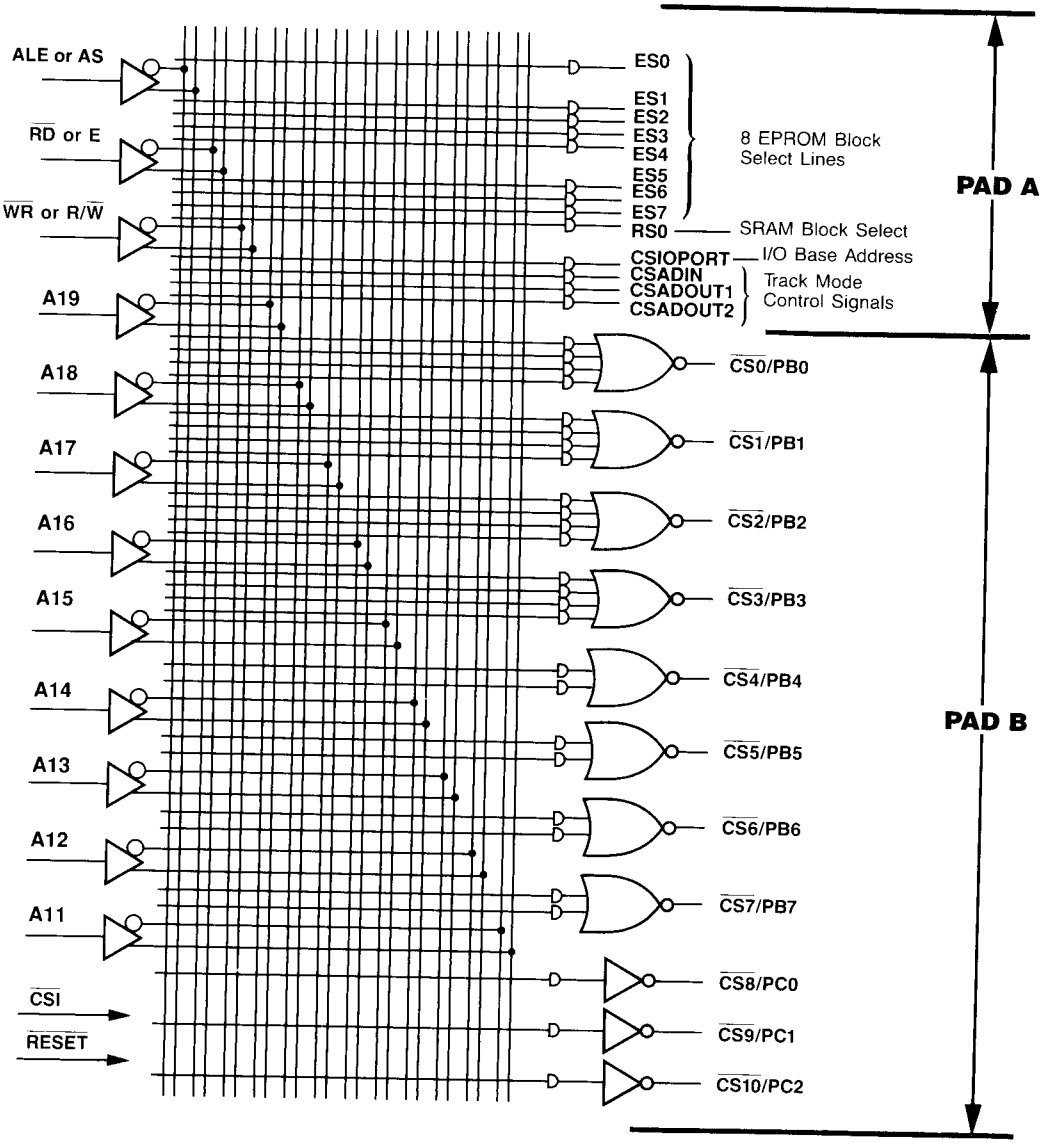
1. PSD311 configured for multiplexed 8-bit address/data bus.
2. PSD311configured for non-multiplexed address/data, 8-bit bus.

Legend: AD0–AD7 = Addresses A0–A7 multiplexed with data lines D0–D7.

Table 2. PSD311 Bus and Port Configuration Options

	Multiplexed Address/Data	Non-Multiplexed Address/Data
8-bit Data Bus		
Port A	I/O or low-order address lines or Low-order multiplexed address/data byte	D0–D7 data bus byte
Port B	I/O or $\overline{CS0}$–$\overline{CS7}$	I/O and/or $\overline{CS0}$–$\overline{CS7}$
AD0/A0–AD7/A7	Low-order multiplexed address/data byte	Low-order address bus byte
A8–A15	High-order address bus byte	High-order address bus byte

Figure 3. PSD311 PAD Description



NOTES: 2. $\overline{CSI}$ is a power-down signal. When high, the PAD is in stand-by mode and all its outputs become non-active. See Tables 10 and 11.
3. RESET deselects all PAD output signals. See Tables 8 and 9.
4. Maximum PAD latency is 35 ns.
5. A18, A17, and A16 are internally multiplexed with $\overline{CS10}$, $\overline{CS9}$, and $\overline{CS8}$, respectively. Either A18 or $\overline{CS10}$, A17 or $\overline{CS9}$, and A10 or $\overline{CS8}$ can be routed to the external pins of Port C.

Table 3. PSD311 PAD A and B I/O Functions

	Function
PAD A and PAD B Inputs	
$\overline{CSI}$ or A19	In $\overline{CSI}$ mode (when high), PAD deselects all of its outputs and enters a power-down mode (see Tables 10 and 11). In A19 mode, it is another input to the PAD.
A16–A18	These are general purpose inputs from Port C. See Figure 3, Note 4.
A11–A15	These are address inputs.
P0–P3	These are page number inputs.
$\overline{RD}$ or E	This is the read pulse or enable strobe input.
$\overline{WR}$ or R/$\overline{W}$	This is the write pulse or R/$\overline{W}$ select signal.
ALE	This is the ALE input to the chip.
RESET	This deselects all outputs from the PAD; it can not be used in product term equations. See Tables 8 and 9.
PAD A Outputs	
ES0–ES7	These are internal chip-selects to the 8 EPROM banks. Each bank can be located on any boundary that is a function of one product term of the PAD address inputs.
RS0	This is an internal chip-select to the SRAM. Its base address location is a function of one term of the PAD address inputs.
CSIOPORT	This internal chip-select selects the I/O ports. It can be placed on any boundary that is a function of one product term of the PAD inputs. See Table 6.
CSADIN	This internal chip-select, when Port A is configured as a low-order address/data bus in the track mode (CPAF2 = 1), controls the input direction of Port A. CSADIN is gated externally to the PAD by the internal read signal. When CSADIN and a read operation are active, data presented on Port A flows out of AD0/A0–AD7/A7. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 5.
CSADOUT1	This internal chip-select, when Port A is configured as a low-order address/data bus in track mode (CPAF2 = 1), controls the output direction of Port A. CSADOUT1 is gated externally to the PAD by the ALE signal. When CSADOUT1 and the ALE signal are active, the address presented on AD0/A0–AD7/A7 flows out of Port A. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 5.
CSADOUT2	This internal chip-select, when Port A is configured as a low-order address/data bus in the track mode (CPAF2 = 1), controls the output direction of Port A. CSADOUT2 must include the write-cycle control signals as part of its product term. When CSADOUT2 is active, the data presented on AD0/A0–AD7/A7 flows out of Port A. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 5.
PAD B Outputs	
$\overline{CS0}$–$\overline{CS3}$	These chip-select outputs can be routed through Port B. Each of them is a function of up to four product terms of the PAD inputs.
$\overline{CS4}$–$\overline{CS7}$	These chip-select outputs can be routed through Port B. Each of them is a function of up to two product terms of the PAD inputs.
$\overline{CS8}$–$\overline{CS10}$	These chip-select outputs can be routed through Port C. See Figure 3, Note 4. Each of them is a function of one product term of the PAD inputs.

Configuration Bits

The configuration bits shown in Table 4 are non-volatile cells that let the user set the device, I/O, and control functions to the proper operational mode. Table 5 lists all configuration bits. The configuration bits are programmed and verified during the programming phase. In operational mode, they are not accessible. To simplify implementing a specific mode, use the WSI's PSD311 MAPLE software to set the bits.

Table 4. PSD311 Non-Volatile Configuration Bits

Use This Bit	To
CADDRDAT	Set the address/data buses to multiplexed or non-multiplexed mode.
CRRWR	Set the $\overline{RD}$/E and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins to $\overline{RD}$ and $\overline{WR}$ pulse, or to E strobe and R/$\overline{W}$ status.
CA19/$\overline{CSI}$	Set A19/$\overline{CSI}$ to $\overline{CSI}$ (power-down) or A19 input.
CALE	Set the ALE polarity.
CPAF2	Set Port A either to track the low-order byte of the address/data multiplexed bus or to select the I/O or address option. (Note 6)
CSECURITY	Set the security on or off.
CRESET	Set the RESET polarity.
$\overline{COMB}$/SEP	Set $\overline{PSEN}$ and $\overline{RD}$ for combined or separate address spaces (see Figures 8 and 9).
CPAF1	Configure each pin of Port A in multiplexed mode to be an I/O or address output.
CPACOD	Configure each pin of Port A as an open drain or active CMOS pull-up output.
CPBF	Configure each pin of Port B as an I/O or a chip-select output.
CPBCOD	Configure each pin of Port B as an open drain or active CMOS pull-up output.
CPCF	Configure each pin of Port C as an address input or a chip-select output.
CADDHLT	Configure pins A16–A19 to go through a latch or to have their latch transparent.
CATD	Configure Pins A16–A19 as PAD logic inputs or higher-order address inputs

NOTE: 6. For functional and value descriptions, refer to Table 5.

Table 5. PSD311 Configuration Bits[7,8] (45 total bits)

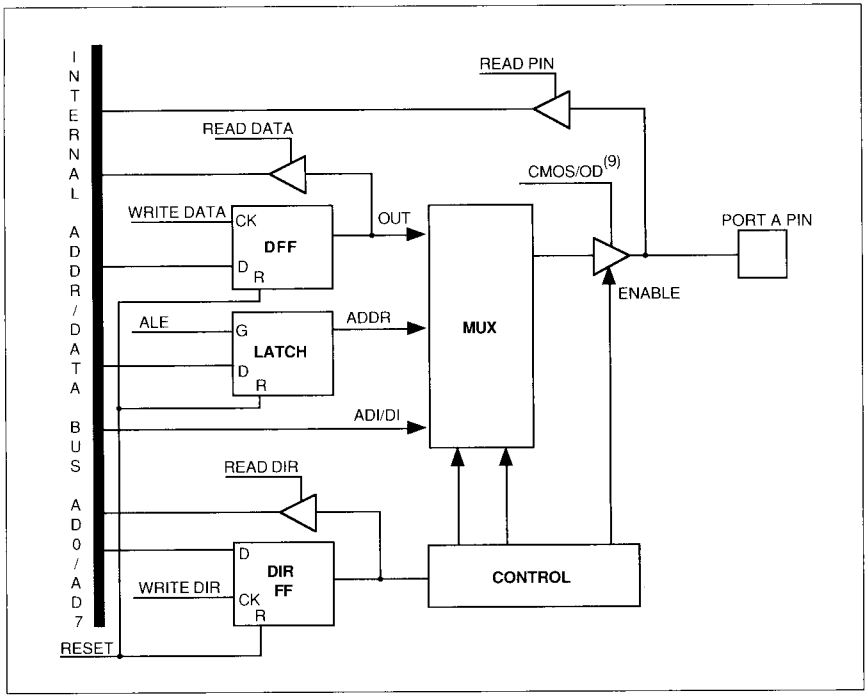
Configuration Bits	No. of Bits	Function
CADDRDAT	1	Address/data multiplexed or non-multiplexed (separate buses) CADDRDAT = 0, non-multiplexed address/data bus CADDRDAT = 1, multiplexed address/data bus
CRRWR	1	CRRWR = 0, $\overline{RD}$ and $\overline{WR}$ active low strobes CRRWR = 1, R/$\overline{W}$ status and E active high pulse
CA19/CSI	1	A19 or $\overline{CSI}$ CA19/$\overline{CSI}$ = 0, enable power-down mode CA19/$\overline{CSI}$ = 1, A19 input to PAD
CALE	1	Active high or active low CALE = 0, active high CALE = 1, active low
CRESET	1	Active high or active low CRESET = 0, active low reset signal CRESET = 1, active high reset signal
$\overline{COMB}$/SEP	1	Combined or separate memory space for EPROM and SRAM $\overline{COMB}$/SEP = 0, combined $\overline{COMB}$/SEP = 1, separate
CPAF1	8	Port A I/Os or A0–A7 CPAF1 = 0, Port A pin = I/O CPAF1 = 1, Port A pin = Ai ($0 \leq i \geq 7$)
CPAF2	1	Port A AD0–AD7 (address/data multiplexed bus) CPAF2 = 0, address or I/O on Port A (according to CPAF1) CPAF2 = 1, address/data multiplexed on Port A (track mode)
CPBF	8	Port B I/Os or $\overline{CS0}$–$\overline{CS7}$ CPBF = 0, Port B Pin = $\overline{CSi}$ ($0 \leq i \leq 7$) CPBF = 1, Port B Pin = I/O
CPCF	3	Port C A16–A18 or $\overline{CS8}$–$\overline{CS10}$ CPCF = 0, Port C Pin = Ai ($16 \leq i \leq 18$) CPCF = 1, Port C Pin = $\overline{CSi}$ ($8 \leq i \leq 10$)
CPACOD	8	Port A CMOS or open-drain outputs CPACOD = 0, CMOS output CPACOD = 1, open-drain output
CPBCOD	8	Port B CMOS or open-drain outputs CPBCOD = 0, CMOS output CPBCOD = 1, open-drain output
CADDHLT	1	A16–A19 latched or latch transparent CADDHLT = 0, address latch transparent CADDHLT = 1, address latched (ALE dependent)
CATD	1	A16–A19 used as address or logic inputs CATD = 0, logic inputs CATD = 1, address inputs
CSECURITY	1	Security on or off CSECURITY = 0, no security CSECURITY = 1, secured part (cannot be copied)

NOTES: 7. WSI's MAPLE software will guide the user to the proper configuration choice.
8. In an unprogrammed or erased part, all configuration bits are 0.

Port Functions

The PSD311 has three I/O ports (Ports A, B, and C) that are configurable at the bit level. This permits great flexibility and a high degree of customization for specific applications. The following is a description of each port. Figure 4 shows the pin structure of Port A.

Figure 4. Port A Pin Structure



NOTE: 9. CMOS/OD determines whether the output is open drain or CMOS.

Port Functions (Cont.)

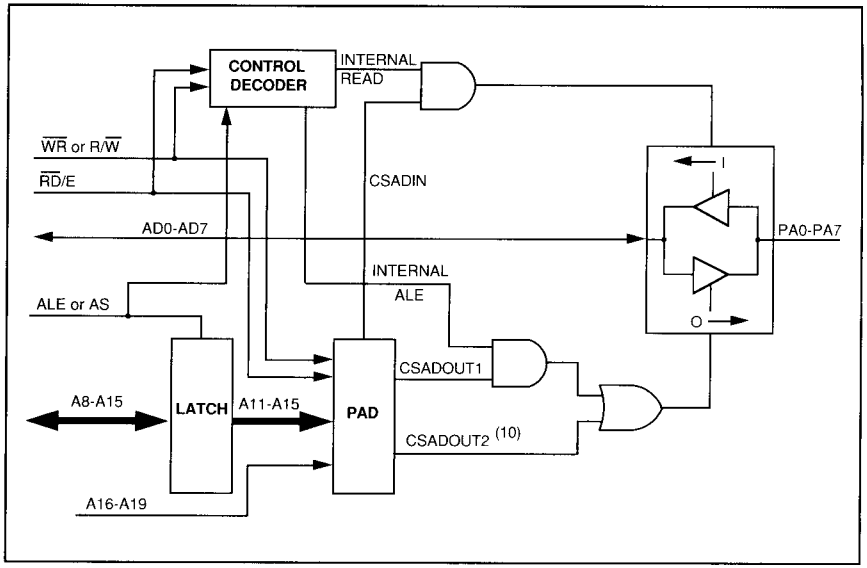
Port A in Multiplexed Address/Data Mode

The default configuration of Port A is I/O. In this mode, every pin can be set as an input or output by writing into the respective pin's direction flip flop (DIR FF, in Figure 4). As an output, the pin level can be controlled by writing into the respective pin's data flip flop (DFF, in Figure 4). When DIR FF = 1, the pin is configured as an output. When DIR FF = 0, the pin is configured as an input. The controller can read the DIR FF bits by accessing the READ DIR register; it can read the DFF bits by accessing the READ DATA register. Port A pin levels can be read by accessing the READ PIN register.

Individual pins can be configured as CMOS or open drain outputs. Open drain pins require external pull-up resistors. For addressing information, refer to Table 6.

Alternatively, each bit of Port A can be configured as a low-order latched address bus bit. The address is provided by the port address latch, which latches the address on the trailing edge of ALE. PA0–PA7 can become A0–A7, respectively. This feature of the PSD311 lets the user generate low-order address bits to access external peripherals or memory that require several low-order address lines.

Figure 5. Port A Track Mode



NOTE: 10. The expression for CSADOUT2 must include the following write operation cycle signals:
For CRRWR = 0, CSADOUT2 must include $\overline{WR}$ = 0.
For CRRWR = 1, CSADOUT2 must include E = 1 and R/$\overline{W}$ = 0.

Port Functions (Cont.)

Another mode of Port A (CPAF2 = 1) sets the entire port to track the inputs AD0/A0–AD7/A7, depending on specific address ranges defined by the PAD's CSADIN, CSADOUT1, and CSADOUT2 signals. This feature lets the user interface the microcontroller to shared external resources without requiring external buffers and decoders. In this mode, the port is effectively a bi-directional buffer. The direction is controlled by using the input signals ALE, $\overline{RD}$/E, $\overline{WR}$/V_{PP} or R/$\overline{W}$, and the internal PAD outputs CSADOUT1, CSADOUT2 and CSADIN (see Figure 5). When CSADOUT1 and ALE are true, the address on the input AD0/A7–AD7/A7 pins flows out through Port A. (Carefully check the generation of CSADOUT1, and ensure that it is stable during the ALE pulse; see Figure 17). When CSADOUT2 is active, a write operation is performed (see note to Figure 5). The data on the input AD0/A7–AD7/A7 pins flows out through Port A. When CSADIN and a read operation is performed (depending on the mode of the $\overline{RD}$/E and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins), the data on Port A flows out through the AD0/A7–AD7/A7 pins. In this operational mode, Port A is tri-stated when none of the above-mentioned three conditions exist.

Port Functions (Cont.)

Port A in Non-Multiplexed Address/Data Mode

In this mode, Port A becomes the low order data bus byte of the chip. When reading an internal PSD311 location, data is presented on Port A pins. When writing to an internal PSD311 location, data present on Port A pins is written to that location.

Port B

The default configuration of Port B is I/O. In this mode, every pin can be set as an input or output by writing into the respective pin's direction flip flop (DIR FF, in Figure 6). As an output, the pin level can be controlled by writing into the respective pin's data flip flop (DFF, in Figure 6). When DIR FF = 1, the pin is configured as an output. When DIR FF = 0, the pin is configured as an input. The controller can read the DIR FF bits by accessing the READ DIR register; it can read the DFF bits by accessing the READ DATA register. Port B pin levels can be read by accessing the READ PIN register. Individual pins can be configured as CMOS or open drain outputs. Open drain pins require external pull-up resistors. For addressing information, refer to Table 6

Alternatively, each bit of Port B can be configured to provide a chip-select output signal from PAD B. PB0–PB7 can provide $\overline{CS0}$–$\overline{CS7}$, respectively. Each of the signals $\overline{CS0}$–$\overline{CS3}$ is comprised of four product terms.Thus, up to four ANDed expressions can be ORed while deriving any of these signals. Each of the signals $\overline{CS4}$–$\overline{CS7}$ is comprised of two product terms. Thus, up to two ANDed expressions can be ORed while deriving any of these signals.

Accessing the I/O Port Registers

Table 6 shows the offset values with the respect to the base address defined by the CSIOPORT. They let the user access the corresponding registers.

Port C in All Modes

Each pin of Port C (shown in Figure 7) can be configured as an input to PAD A and PAD B or output from PAD B. As inputs, the pins are named A16–A18. Although the pins are given names of the high-order address bus, they can be used for any other address lines or logic inputs to PAD A and PAD B. For example, A8–A10 can also be connected to those pins, improving the boundaries of $\overline{CS0}$–$\overline{CS7}$ resolution to 256 bytes. As inputs, they can be individually configured to be logic or address inputs. A logic input uses the PAD only for Boolean equations that are implemented in any or all of the $\overline{CS0}$–$\overline{CS10}$ PAD B outputs. Port C addresses can be programmed to latch the inputs by the trailing edge ALE or to be transparent.

Alternatively, PC0–PC2 can become $\overline{CS8}$–$\overline{CS10}$ outputs, respectively, providing the user with more external chip-select PAD outputs. Each of the signals $\overline{CS8}$–$\overline{CS10}$ is comprised of one product term.

ALE/AS and AD0/A0–AD7/A7 in Non-Multiplexed Modes

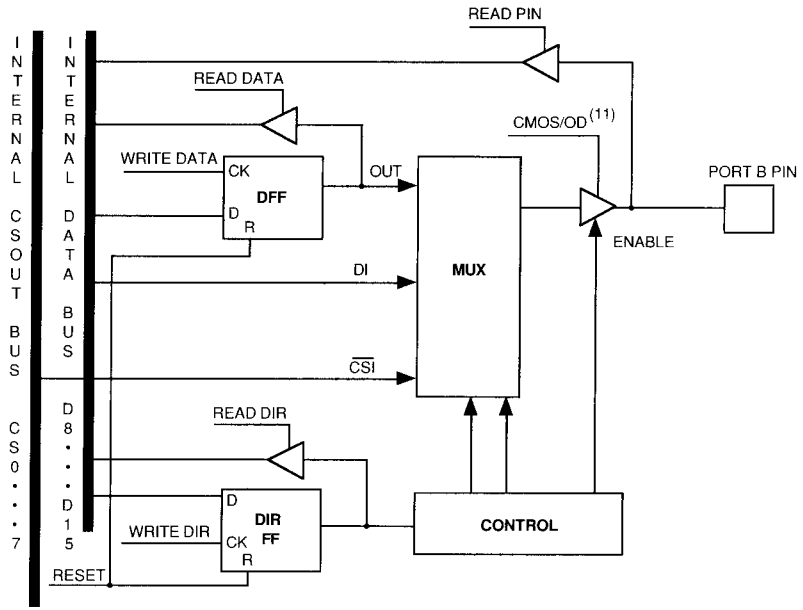
In non-multiplexed modes, A0–A15 are address inputs only and can become transparent (CLOT = 0) or ALE dependent (CLOT = 1). In transparent mode, the ALE/AS pin can be used as an additional logic input to the PADs. The non-multiplexed ALE dependent mode is useful in applications for which the host processor has a multiplex address/data bus and AD0/A0–AD7/A7 are not multiplexed with A0–A7 but rather are multiplexed with other address lines. In these applications, Port A serves as a data bus and each of its pins can be directly connected to the corresponding host's multiplexed pin, where that data bit is expected. See Table 7.

A16–A19 As Inputs

If one or more of the pins PC0, PC1, PC2 and $\overline{CSI}$/A19 are configured as inputs, the configuration bits CADDHLT and CATD define their functionality inside the part. CADDHLT determines if these inputs are to be latched by the trailing edge of the ALE or AS signal (CADDHLT = 1), or enabled into the PSD311 at all times (CADDHLT = 0), transparent mode). CATD determines whether these lines are high-order address lines, that take part in the derivation of memory and I/O select signals inside the chip (CATD = 1), or logic input lines that have no impact on memory or I/O selections (CATD = 0). Logic input lines typically participate in the Boolean expressions implemented in the PAD.

Figure 6. Port B Pin Structure

Figure 6 shows the structure of Port B.

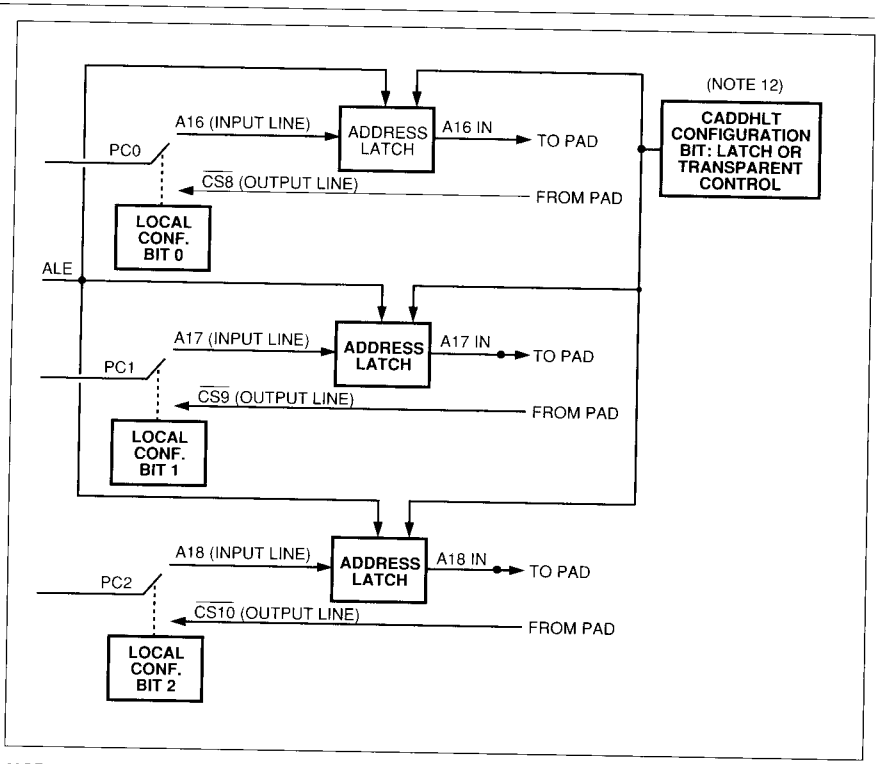


NOTE: 11. CMOS/OD determines whether the output is open drain or CMOS.

Table 6. I/O Port Addresses

Register Name	Byte Size Access of the I/O Port Registers Offset from the CSIOPORT
Pin Register of Port A	+ 2 (accessible during read operation only)
Direction Register of Port A	+ 4
Data Register of Port A	+ 6
Pin Register of Port B	+ 3 (accessible during read operation only)
Direction Register of Port B	+ 5
Data Register of Port B	+ 7

Figure 7. Port C Structure



NOTE: 12. The CADDHLT configuration bit determines if A18–A16 are transparent via the latch, or if they must be latched by the trailing edge of the ALE strobe.

Table 7. Signal Latch Status in All Operating Modes

Signal Name	Configuration Bits	Configuration Mode	Signal Latch Status
AD0/A0-AD7/A7	CADDRDAT = 0	non-multiplexed mode	Transparent
	CADDRDAT = 1	multiplexed modes	ALE Dependent
$\overline{PSEN}$	CDATA = 0	8-bit data, $\overline{PSEN}$ is active	Transparent
A19 and PC2–PC0	CADDHLT = 0	A16–A19 can become logic inputs	Transparent
	CADDHLT = 1	A16–A19 can become multiplexed address lines	ALE Dependent

EPROM

The PSD311 has 256K bits of EPROM and is organized as 32K x 8. The EPROM has 8 banks of memory. Each bank can be placed in any address location by programming the PAD. Bank0–Bank7 can be selected by PAD outputs ES0–ES7, respectively. The EPROM banks are organized as 4K x 8.

SRAM

The PSD311 has 16K bits of SRAM and is organized as 2K x 8. The SRAM is selected by the RS0 output of the PAD.

Control Signals

The PSD311 control signals are $\overline{WR}/V_{PP}$ or R/$\overline{W}$, $\overline{RD}$/E, ALE, $\overline{PSEN}$, Reset, and A19/$\overline{CSI}$. Each of these signals can be configured to meet the output control signal requirements of various microcontrollers.

$\overline{WR}/V_{PP}$ or R/$\overline{W}$

In operational mode, this signal can be configured as $\overline{WR}$ or R/$\overline{W}$. As $\overline{WR}$, all write operations to the PSD311 are activated by an active low signal on this pin. As R/$\overline{W}$, the pin works with the E strobe of the $\overline{RD}$/E pin. When R/$\overline{W}$ is high, an active high signal on the $\overline{RD}$/E pin performs a read operation. When R/$\overline{W}$ is low, an active high signal on the $\overline{RD}$/E pin performs a write operation.

$\overline{RD}$/E

In operational mode, this signal can be configured as $\overline{RD}$, or E. As $\overline{RD}$, all read operations to the PSD311 are activated by an active low signal on this pin. As E, the pin works with the R/$\overline{W}$ strobe of the $\overline{WR}/V_{PP}$ or R/$\overline{W}$ pin. When R/$\overline{W}$ is high, an active high signal on the $\overline{RD}$/E pin performs a read operation. When R/$\overline{W}$ is low, an active high signal on the $\overline{RD}$/E pin performs a write operation.

ALE or AS

ALE polarity is programmable. When programmed to be active high, a high on the pin causes the input address latches, Port A address latches, Port C, and A19 address latches to be transparent. The falling edge of ALE locks the information into the latches. When ALE is programmed to be active low, a low on the pin causes the input address latches, Port A address latches, Port C, and A19 address latches to be transparent. The rising edge of ALE locks the appropriate information into the latches.

$\overline{PSEN}$

The $\overline{PSEN}$ function enables the user to work with two address spaces: program memory and data memory (if $\overline{COMB}$/SEP = 1). In this mode, an active low signal on the $\overline{PSEN}$ pin causes the EPROM to be read. The SRAM and I/O ports read operation are done by $\overline{RD}$ low (CRRWR = 0), or by E and R/$\overline{W}$ high (CRRWR = 1).

Control Signals (Cont.)

Whenever a member of the 8031 family (or any other similar microcontroller) is used, the PSD311's $\overline{PSEN}$ pin must be connected to the $\overline{PSEN}$ pin of the microcontroller.

If $\overline{COMB}$/SEP = 0, the address spaces of the program and the data are combined. In this configuration (except for the 8031-type case mentioned above), the $\overline{PSEN}$ pin must be tied high to V_{CC}, and the EPROM, SRAM, and I/O ports are read by $\overline{RD}$ low (CRRWR = 0), or by E and R/$\overline{W}$ high (CRRWR = 1). See Figures 8 and 9.

Figure 8. Combined Address Space

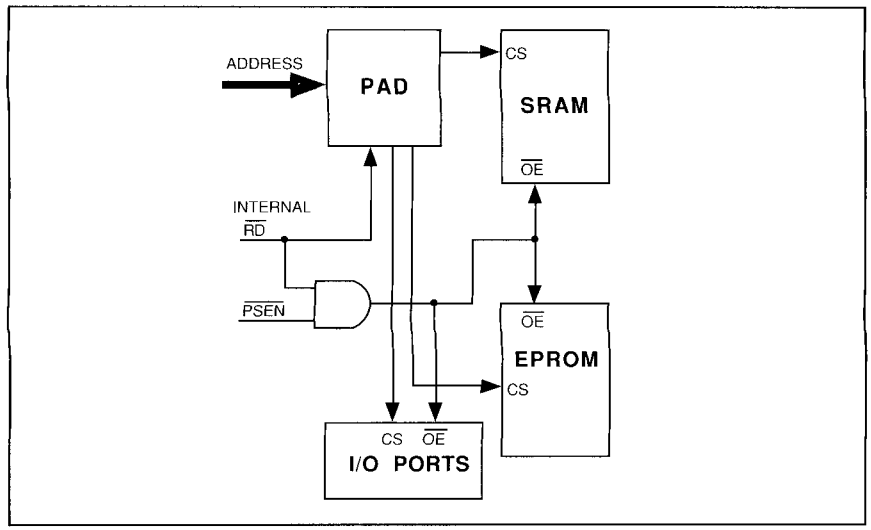
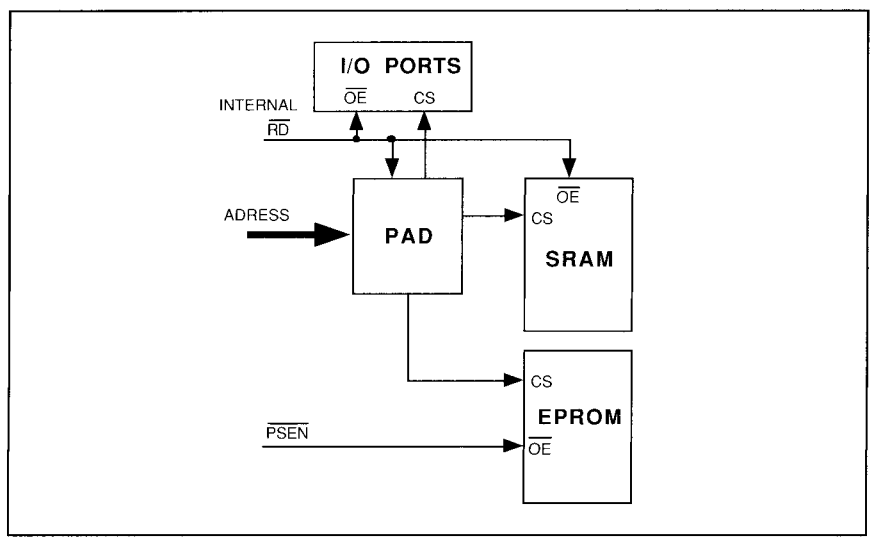


Figure 9. 8031-Type Separate Code and Data Address Spaces



Control Signals (Cont.)

RESET

This is an asynchronous input pin that clears and initializes the PSD311. Reset polarity is programmable (active low or active high). Whenever the PSD311 reset input is driven active for at least 100 ns, the chip is reset. During boot-up (V_{CC} applied), the device is automatically reset internally (internal automatic reset is over by the time V_{CC} operating range has been achieved during boot-up). Tables 8 and 9 indicate the state of the part during and after reset.

A19/CSI

When configured as CSI, a high on this pin deselects, and powers down, the chip. A low on this pin puts the chip in normal operational mode. For PSD311 states during the power-down mode, see Tables 10 and 11, and Figure 10.

In A19 mode, the pin is an additional input to the PAD. It can be used as an address line (CADDHLT = 1) or as a general-purpose logic input (CADDHLT = 0). A19 can be configured as ALE dependent or as transparent input (see Table 7). In this mode, the chip is always enabled.

Table 8. Signal States During and After Reset

Signal	Configuration Mode	Condition
AD0/A0–AD7/A7	All	Input
A8–A15	All	Input
PA0–PA7) (Port A	I/O Tracking AD0/A0–AD7 Address outputs A0–A7	Input Input Low
PB0–PB7 (Port B)	I/O $\overline{CS7}$–$\overline{CS0}$ CMOS outputs $\overline{CS7}$–$\overline{CS0}$ open drain outputs	Input High Tri-stated
PC0–PC2 (Port C)	Address inputs A16–A18 $\overline{CS8}$–$\overline{CS10}$ CMOS outputs	Input High

Table 9. Internal States During and After Reset

Component	Signals	Contents
PAD	$\overline{CS0}$–$\overline{CS10}$	All = 1 (Note 13)
	CSADIN, CSADOUT1, CSADOUT2, CSIOPORT, RS0, ES0–ES7	All = 0 (Note 13)
Data register A Direction register A Data register B Direction register B	n/a n/a n/a n/a	0 0 0 0

NOTE: 13. All PAD outputs are in a non-active state.

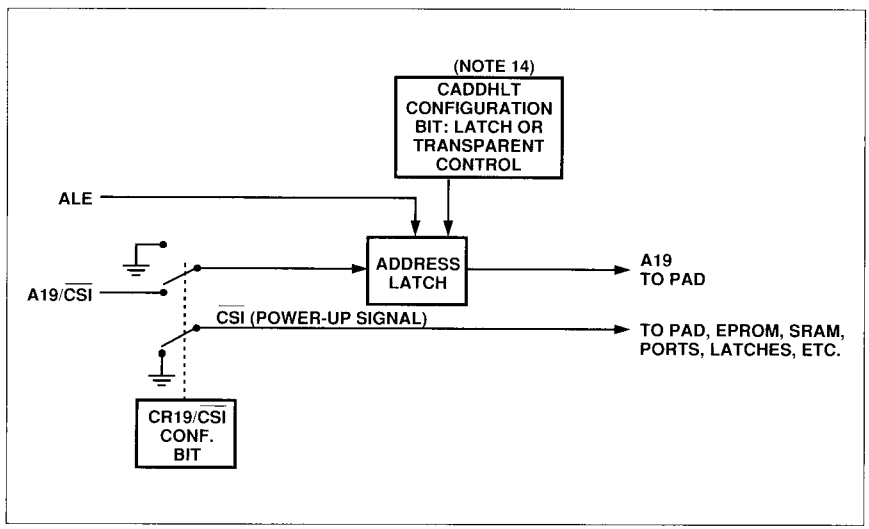
Table 10. Signal States During Power-Down Mode

Signal	Configuration Mode	Condition
AD0/A0–AD7/A7	All	Input
A8–A15	All	Input
PA0–PA7	I/O Tracking AD0/A0–AD7/A7 Address outputs A0–A7	Unchanged Input All 1's
PB0–PB7	I/O $\overline{CS0}$–$\overline{CS7}$ CMOS outputs $\overline{CS0}$–$\overline{CS7}$ open drain outputs	Unchanged All 1's Tri-stated
PC0–PC2	Address inputs A18–A16 $\overline{CS8}$–$\overline{CS10}$ CMOS outputs	Input All 1's

Table 11. Internal States During Power-Down

Component	Signals	Contents
PAD	$\overline{CS0}$–$\overline{CS10}$	All 1's (deselected)
	CSADIN, CSADOUT1, CSADOUT2, CSIOPORT, RS0, ES0–ES7	All 0's (deselected)
Data register A Direction register A Data register B Direction register B	n/a n/a n/a n/a	All unchanged

Figure 10. A19/$\overline{CSI}$ Cell Structure

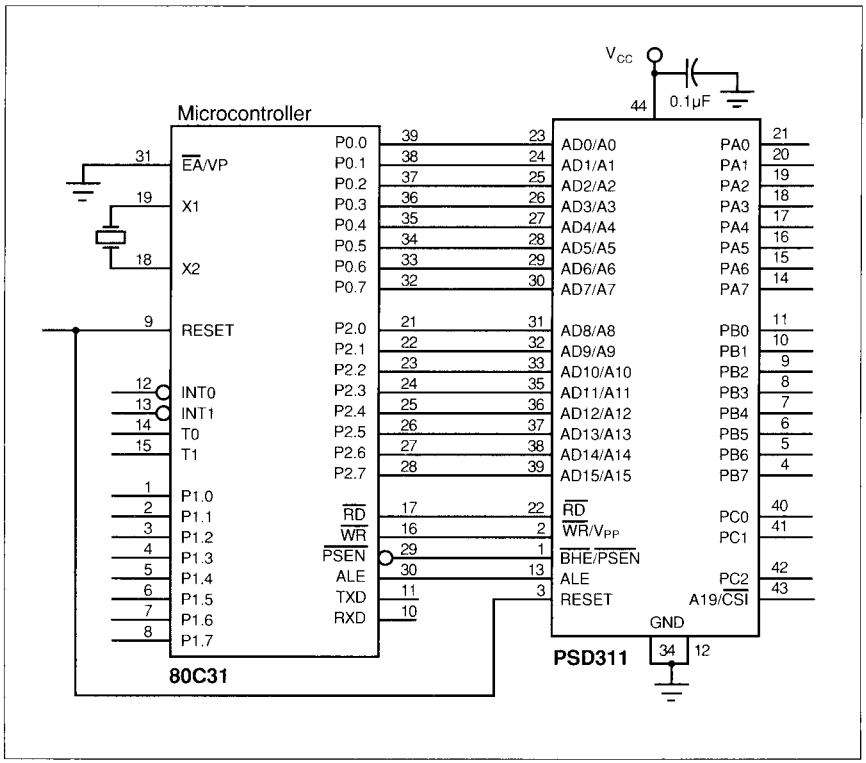


NOTE: 14. The CADDHLT configuration bit determines if A19–A16 are transparent via the latch, or if they must be latched by the trailing edge of the ALE strobe.

System Applications

In Figure 11, the PSD311 is configured to interface with Intel's 80C31, which is a 16-bit address/8-bit data bus microcontroller. Its data bus is multiplexed with the low-order address byte. The 80C31 uses signals $\overline{RD}$ to read from data memory and $\overline{PSEN}$ to read from code memory. It uses $\overline{WR}$ to write into the data memory. It also uses active high reset and ALE signals. The rest of the configuration bits as well as the unconnected signals (not shown) are application specific and, thus, user dependent.

Figure 11. PSD311 Interface With Intel's 80C31



The configuration bits for Figure 11 are:

CRESET	1	COMB/SEP	0 or 1 (both valid)
CALE	0	CRRWR	0
CDATA	0	CEDS	0
CADDRDAT	1		

All other configuration bits may vary according to the application requirements.

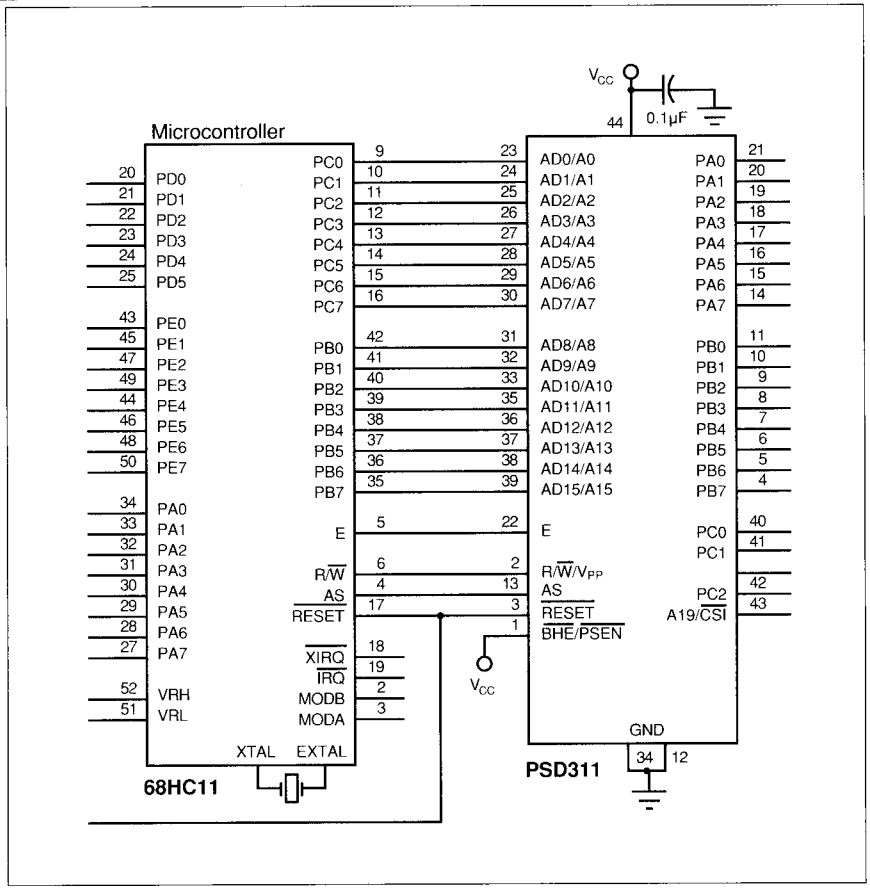
Security Mode

Security Mode in the PSD311 locks the contents of the PAD A , PAD B and all the configuration bits. The EPROM SRAM, and I/O contents can be accessed only through the PAD. The Security Mode can be set by the MAPLE or Programming software. In window packages, the mode is erasable through UV full part erasure. In the security mode, the PSD311 contents cannot be copied on a programmer.

System Applications

In Figure 12, the PSD311 is configured to interface with Motorola's 68HC11, which is a 16-bit address/8-bit data bus microcontroller. Its data bus is multiplexed with the low-order address byte. The 68HC11 uses E and R/W signals to derive the read and write strobes. It uses the term AS (address strobe) for the address latch pulse. RESET is an active low signal. The rest of the configuration bits as well as the unconnected signals (not shown) are application specific and, thus, user dependent.

Figure 12. PSD311 Interface With Motorola's 68HC11



The configuration bits for Figure 12 are:

CRESET	0	COMB/SEP	0
CALE	0	CRRWR	1
CDATA	0	CEDS	0
CADDRDAT	1		

All other configuration bits may vary according to the application requirements.

Absolute Maximum Ratings[15]

Symbol	Parameter	Condition	Min	Max	Unit
T_{STG}	Storage Temperature		– 65	+ 150	°C
	Voltage on any Pin	With Respect to GND	– 0.6	+ 7	V
V_{PP}	Programming Supply Voltage	With Respect to GND	– 0.6	+ 14	V
V_{CC}	Supply Voltage	With Respect to GND	– 0.6	+ 7	V
	ESD Protection			>2000	V

NOTE: 15. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at theses or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Operating Range

Range	Temperature	V_{CC}	Tolerance		
			-12	-15	-20
Commercial	0° C to +70°C	+ 5 V	± 5%	± 10%	± 10%
Industrial	–40°C to +80°C	+ 5 V		± 10%	± 10%
Military	–55°C to +125°C	+ 5 V		± 10%	± 10%

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	-12 Version	4.75	5	5.25	V
V_{CC}	Supply Voltage	-15/-20 Versions	4.5	5	5.5	V
V_{IH}	High-level Input Voltage	V_{CC} = 4.5 V to 5.5 V	2			V
V_{IL}	Low-level Input Voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	V

DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	Output Low Voltage	I_{OL} = 20 µA V_{CC} = 4.5 V		0.01	0.1	V
		I_{OL} = 8 mA V_{CC} = 4.5 V		0.15	0.45	
V_{OH}	Output High Voltage	I_{OH} = –20 µA V_{CC} = 4.5 V	4.4	4.49		V
		I_{OH} = –2 mA V_{CC} = 4.5 V	2.4	3.9		
I_{SB1}	V_{CC} Standby Current (CMOS) (Notes 16 and 18)	Comm'l		50	100	µA
		Ind/Mil		75	150	
I_{SB2}	V_{CC} Standby Current (TTL) (Notes 17 and 18)	Comm'l		1.5	3	mA
		Ind/Mil		2	3.2	
I_{CC1}	Active Current (CMOS) (SRAM Not Selected) (Notes 16 and 19)	Comm'l (Note 20)		16	35	mA
		Comm'l (Note 21)		28	50	
		Ind/Mil (Notes 20)		16	45	
		Ind/Mil (Notes 21)		28	60	

DC Characteristics (Cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC2}	Active Current (CMOS) (SRAM Block Selected) (Notes 16 and 19)	Comm'l (Note 20)		47	80	mA
		Comm'l (Note 21)		59	95	
		Ind/Mil (Note 20)		47	100	
		Ind/Mil (Note 21)		59	115	
I_{CC3}	Active Current (TTL) (SRAM Not Selected) (Notes 17 and 19)	Comm'l (Note 20)		36	65	mA
		Comm'l (Note 21)		58	80	
		Ind/Mil (Note 20)		36	80	
		Ind/Mil (Note 21)		58	95	
I_{CC4}	Active Current (TTL) (SRAM Block Selected) (Notes 17 and 19)	Comm'l (Note 20)		67	105	mA
		Comm'l (Note 21)		79	120	
		Ind/Mil (Note 20)		67	130	
		Ind/Mil (Note 21)		79	145	
I_{LI}	Input Leakage Current	V_{IN} = 5.5 V or GND	–1	± 0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or GND	–10	± 5	10	

NOTE: 16. CMOS inputs: GND ± 0.3 V or V_{CC} ± 0.3V.
17. TTL inputs: $V_{IL} \leq 0.8$ V, $V_{IH} \geq 2.0$ V.
18. $\overline{CSI}$/A19 is high and the part is in a power-down configuration mode.
19. AC power component is 3.0 mA/MHz (power = AC + DC).
20. Ten (10) PAD product terms active. (Add 380 µA per product term, typical, or 480 µA per product term maximum.)
21. Forty-one (41) PAD product terms active.

AC Characteristics (See Timing Diagrams)

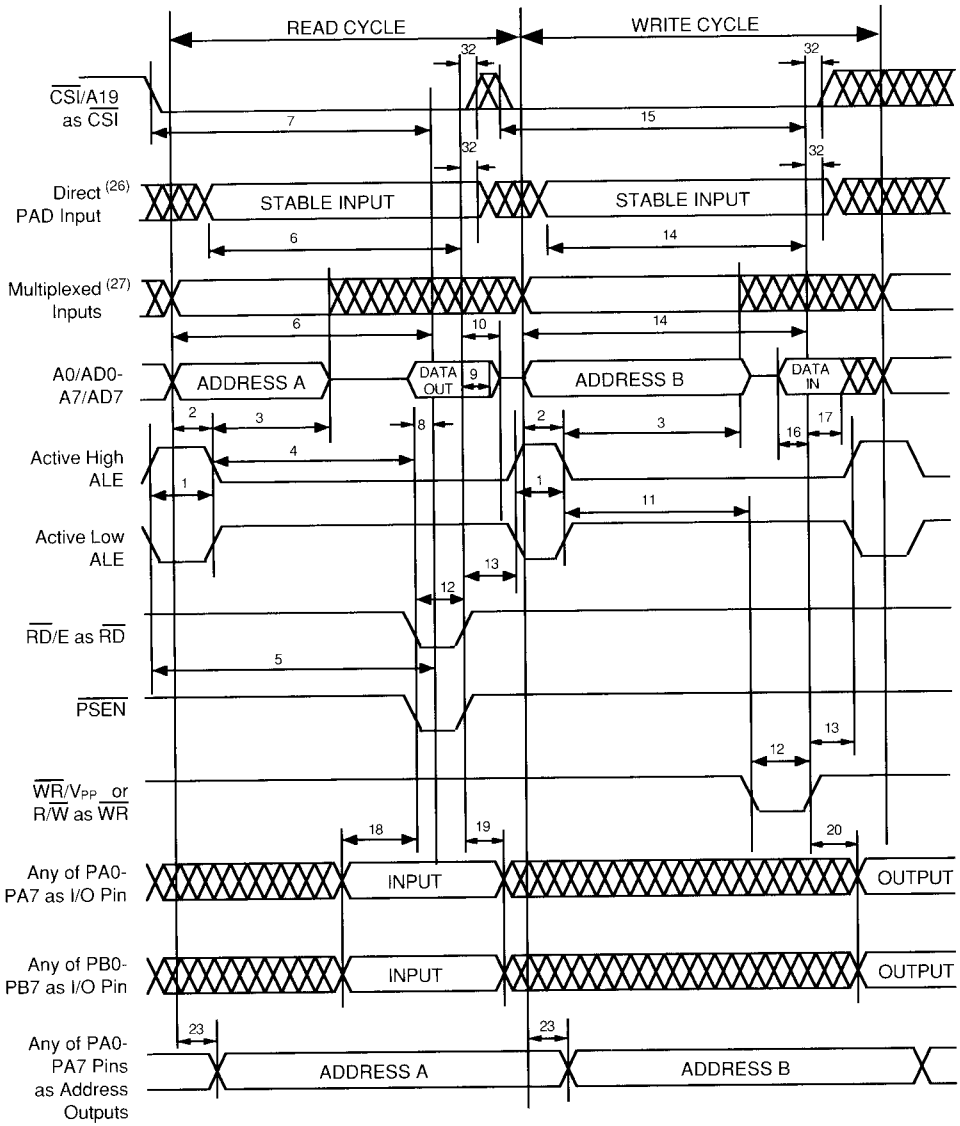
Symbol	Parameter	-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	
T1	ALE or AS Pulse Width	30		40		50		ns
T2	Address Set-up Time	5		10		15		
T3	Address Hold Time	13		15		25		
T4	ALE or AS Trailing Edge to Leading Edge of Read	12		15		20		
T5	ALE Valid to Data Valid	140		170		220		
T6	Address Valid to Data Valid		120		150		200	
T7	$\overline{CSI}$ Active to Data Valid		150		160		200	
T8	Leading Edge of Read to Data Valid		38		55		60	
T9	Read Data Hold Time	0		0		0		
T10	Trailing Edge of Read to Data High-Z		35		40		45	
T11	Trailing Edge of ALE or AS to Leading Edge of Write	12		15		20		
T12	$\overline{RD}$, E, $\overline{PSEN}$ Pulse Width	45		60		75		
T12A	$\overline{WR}$ Pulse Width	25		35		45		
T13	Trailing Edge of Write or Read to Leading Edge of ALE or AS	20		30		40		
T14	Address Valid to Trailing Edge of Write	120		150		200		

AC Characteristics (Cont.)

Symbol	Parameter	-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	
T15	$\overline{CSI}$ Active to Trailing Edge of Write	130		160		210		ns
T16	Write Data Set-up Time	20		30		40		
T17	Write Data Hold Time	5		10		15		
T18	Port Input Set-up Time	30		35		45		
T19	Port Input Hold Time	0		0		0		
T20	Trailing Edge of Write to Port Output Valid	40		50		60		
T21	ADi or Control to $\overline{CSOi}$ Valid	6	35	6	35	5	45	
T22	ADi or Control to $\overline{CSOi}$ Invalid	5	35	4	35	4	45	
T23	Track Mode Address Propagation Delay: CSADOUT1 Already True		22		22		28	
T23A	Track Mode Address Propagation Delay: CSADOUT1 Becomes True During ALE or AS		33		40		50	
T24	Track Mode Address Holding Time	15		15		27		
T25	Track Mode Read Propagation Delay		29		29		35	
T26	Track Mode Read Hold Time	11	29	10	29	10	35	
T27	Track Mode Write Cycle Data Propagation Delay		20		20		30	
T28	Track Mode Write Cycle Write to Data Propagation Delay	8	30	7	40	7	55	
T29	Hold Time of Port A Valid During Write $\overline{CSOi}$ Trailing Edge	2		4		4		
T30	$\overline{CSI}$ Active to $\overline{CSOi}$ Active	9	45	9	45	8	60	
T31	$\overline{CSI}$ Inactive to $\overline{CSOi}$ Inactive	9	45	9	45	8	60	
T32	Direct PAD Input as Hold Time	10		12		15		
T33	R/$\overline{W}$ Active to E or $\overline{DS}$ Start	20		30		40		
T34	E or End to R/$\overline{W}$	20		30		40		
T35	AS Inactive to E High	15		20		25		

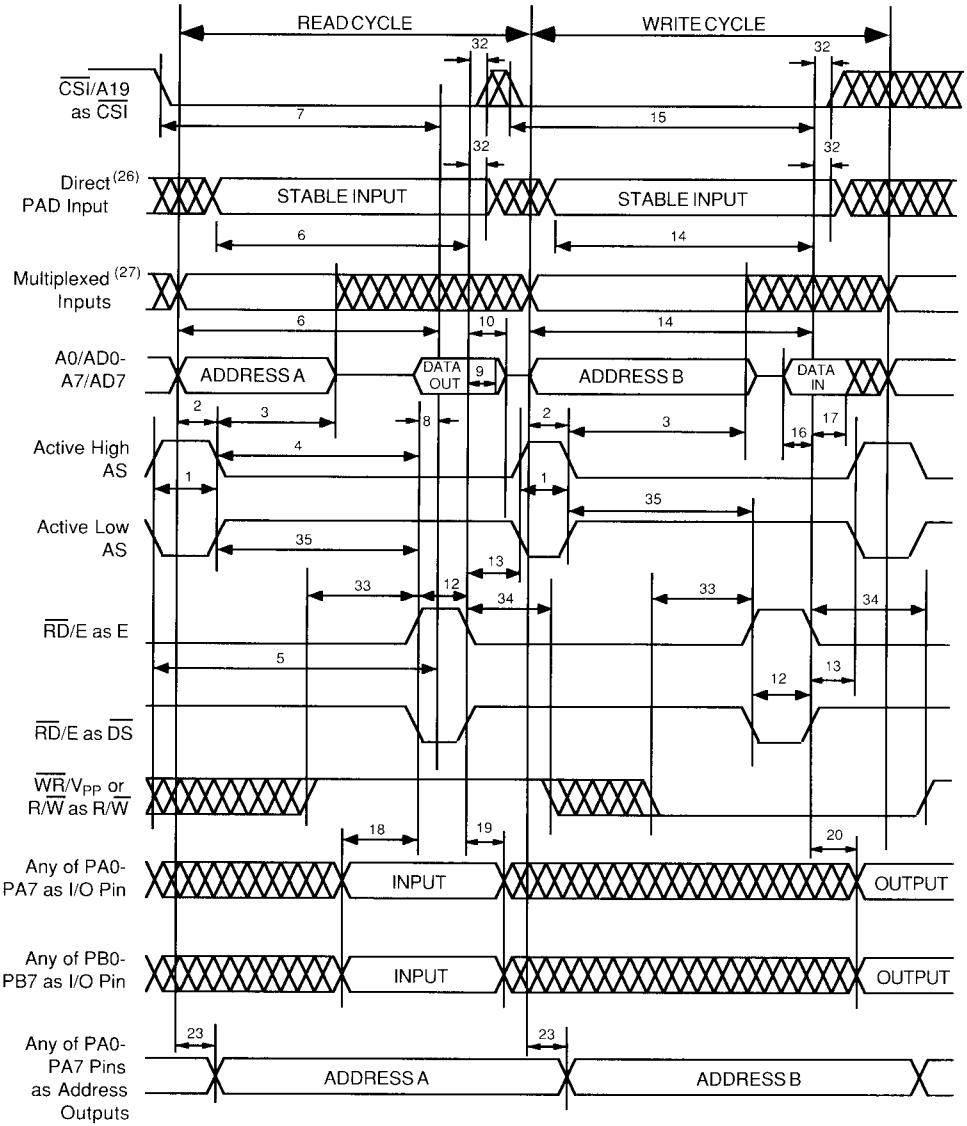
NOTES: 22. ADi = any address line.
23. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
24. Direct PAD input = any of the following direct PAD input lines: CSI/A19 as transparent A19, $\overline{RD}$/E, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE (or AS).
25. Control signals $\overline{RD}$/E or $\overline{WR}$ or R/$\overline{W}$.

Figure 13. Timing of 8-Bit Multiplexed Address/Data Bus, CRRWR = 0



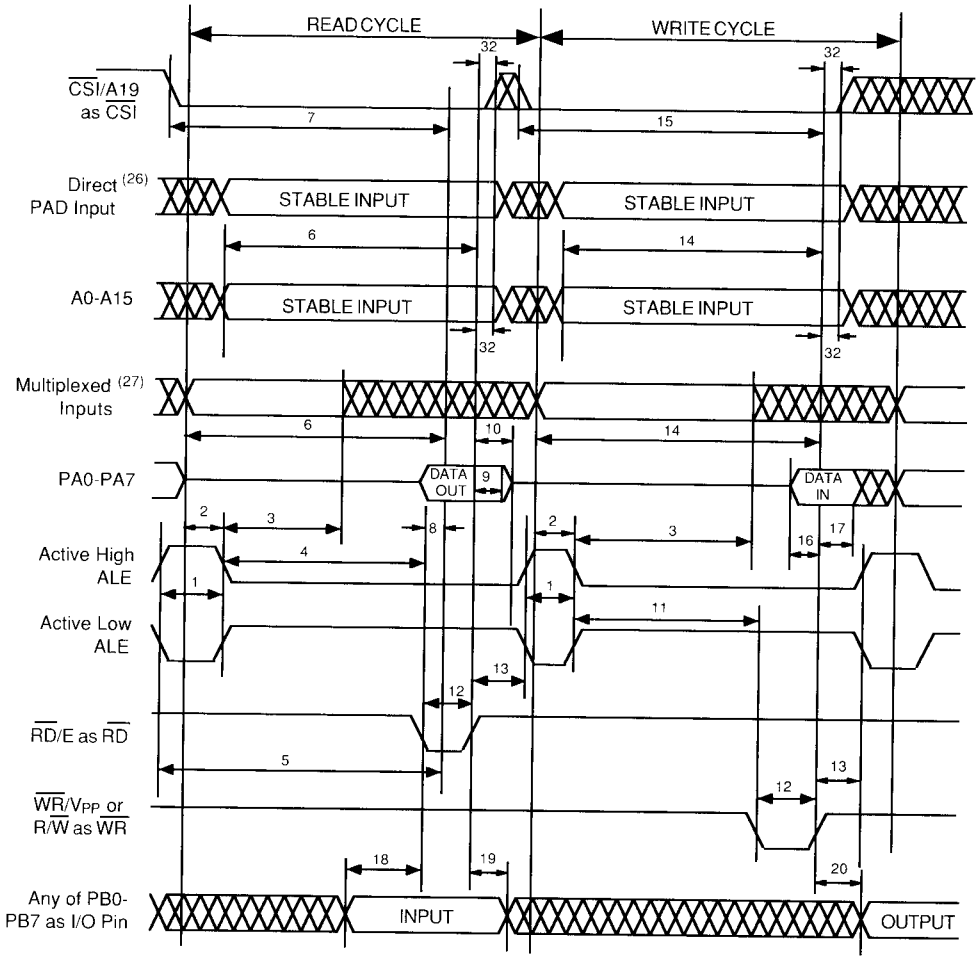
See referenced notes on page 2-75.

Figure 14. Timing of 8-Bit Multiplexed Address/Data Bus, CRRWR = 1



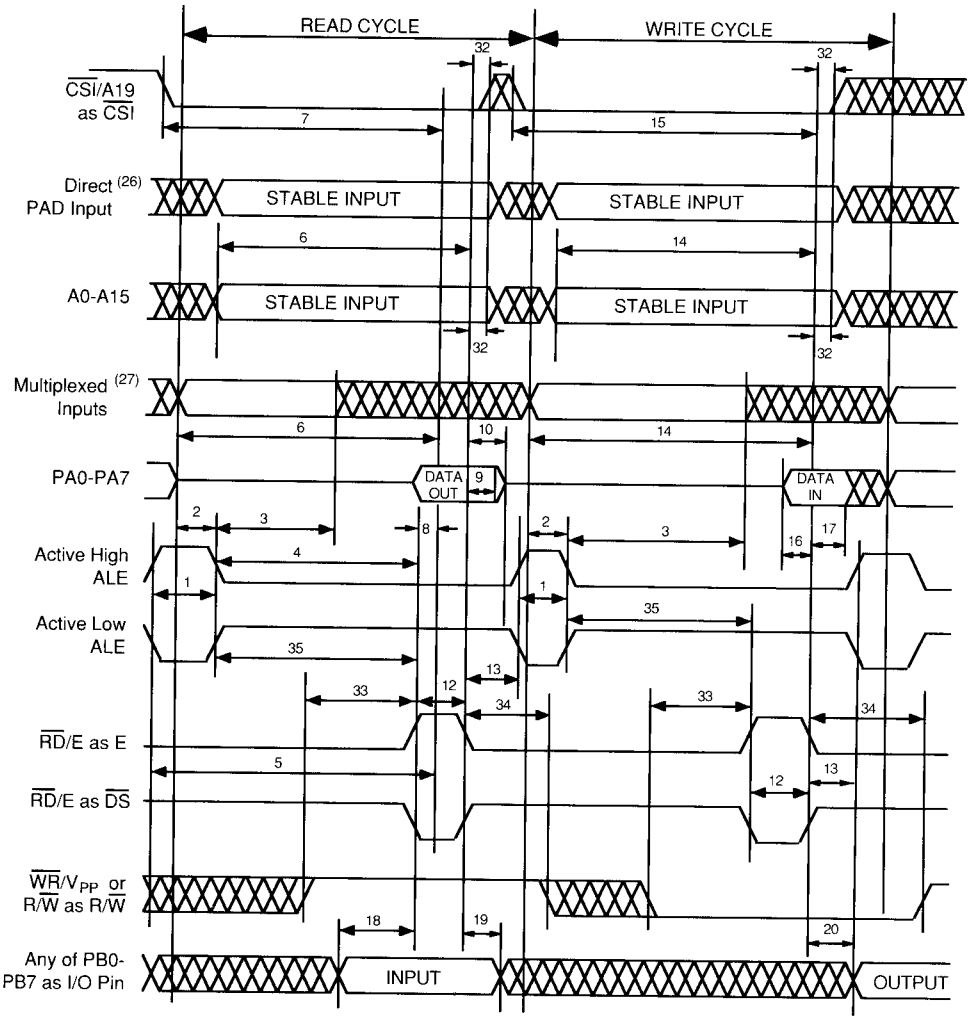
See referenced notes on page 2-75.

Figure 15. Timing of 8-Bit Data Non-Multiplexed Address/Data Bus, CRRWR = 0



See referenced notes on page 2-75.

Figure 16 Timing of 8-Bit Data Non-Multiplexed Address/Data Bus, CRRWR = 1



See referenced notes on page 2-75.

Figure 17. Chip-Select Output Timing

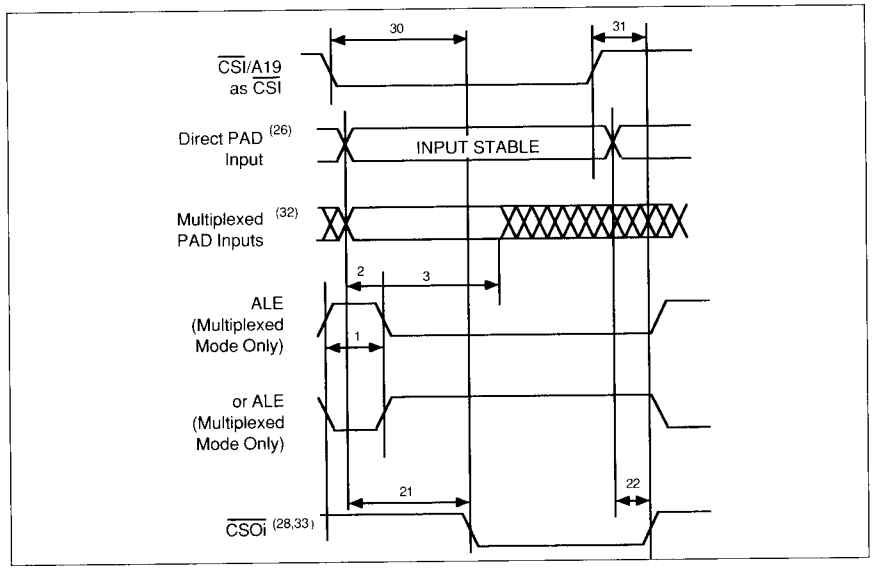
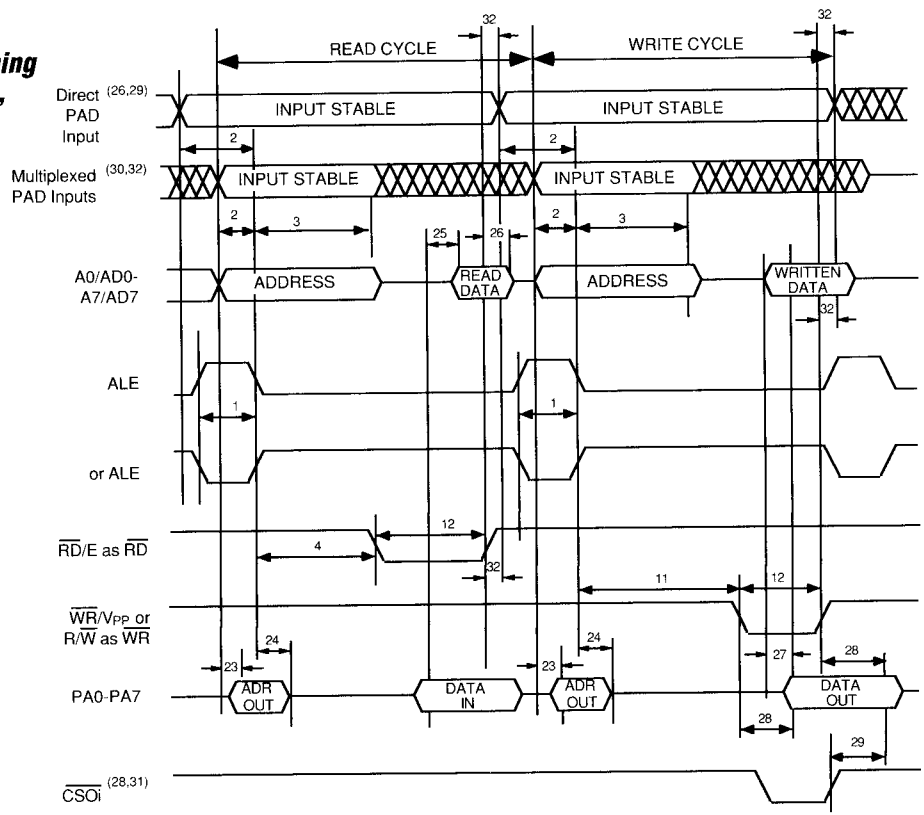
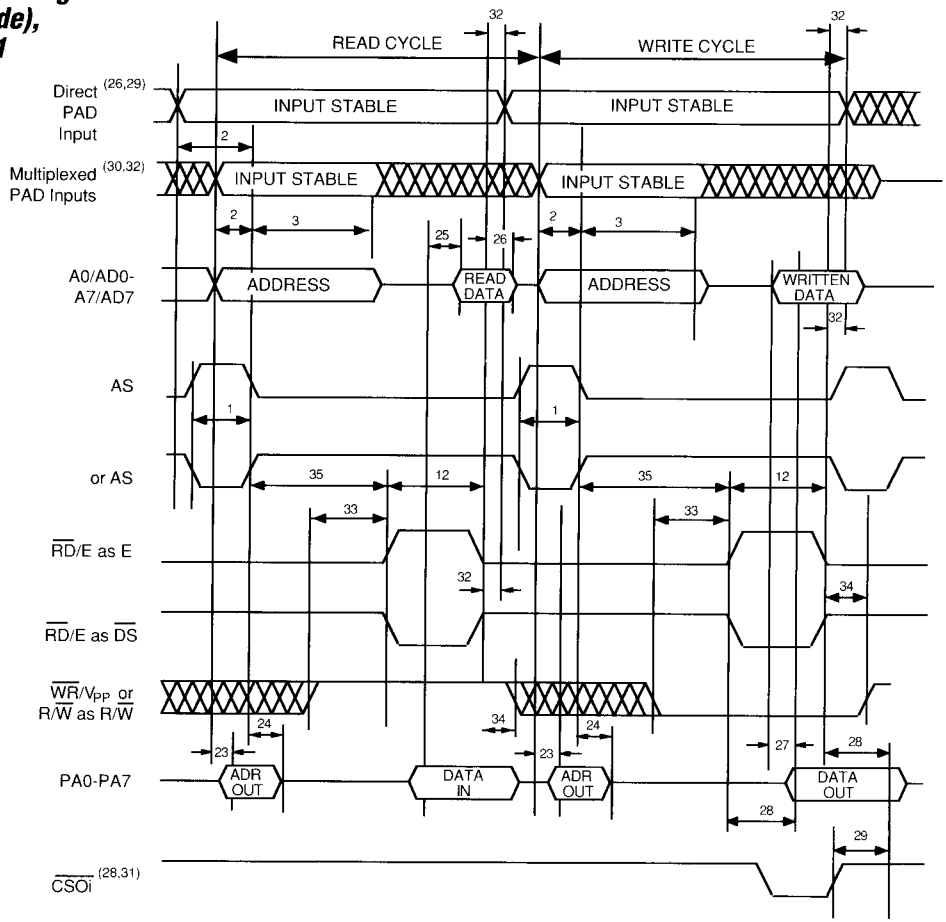


Figure 18. Port A as AD0–AD7 Timing (Track Mode), CRRWR = 0



See referenced notes on page 2-75.

Figure 19. Port A as AD0–AD7 Timing (Track Mode), CRRWR = 1



Notes for Timing Diagrams

26. Direct PAD input = any of the following direct PAD input lines: CSI/A19 as transparent A19, RD/E, WR or R/W, transparent PC0–PC2, ALE in non-multiplexed modes.
27. Multiplexed inputs: any of the following inputs that are latched by the ALE (or AS): A0/AD0–A7/AD7, CSI/A19 as ALE dependent A19, ALE dependent PC0–PC2.
28. CSOi = any of the chip-select output signals coming through Port B (CS0–CS7) or through Port C (CS8–CS10).
29. CSADOUT1, which internally enables the address transfer to Port A, should be derived only from direct PAD input signals, otherwise the address propagation delay is slowed down.
30. CSADIN and CSADOUT2, which internally enable the data-in or data-out transfers, respectively, can be derived from any combination of direct PAD inputs and multiplexed PAD inputs.
31. The write operation signals are included in the CSOi expression.
32. Multiplexed PAD inputs: any of the following PAD inputs that are latched by the ALE (or AS) in the multiplexed modes: A11–A15, CSI/A19 as ALE dependent A19, ALE dependent PC0–PC2.
33. CSOi product terms can include any of the PAD input signals shown in Figure 3, except for reset and CSI.

Table 12 Pin Capacitance[34]

$T_A = 25\,°C$, $f = 1$ MHz

Symbol	Parameter	Conditions	Typical[35]	Max	Units
C_{IN}	Capacitance (for input pins only)	$V_{IN} = 0$ V	4	6	pF
C_{OUT}	Capacitance (for input/output pins)	$V_{OUT} = 0$ V	8	12	pF
C_{VPP}	Capacitance (for $\overline{WR}/V_{PP}$ or $R/\overline{W}/V_{PP}$)	$V_{PP} = 0$ V	18	25	pF

NOTES: 34. This parameter is only sampled and is not 100% tested.
35. Typical values are for $T_A = 25°C$ and nominal supply voltages.

Figure 20. AC Testing Input/Output Waveform

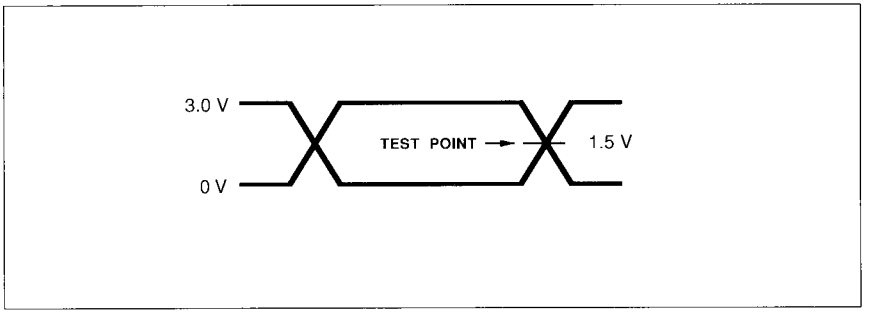
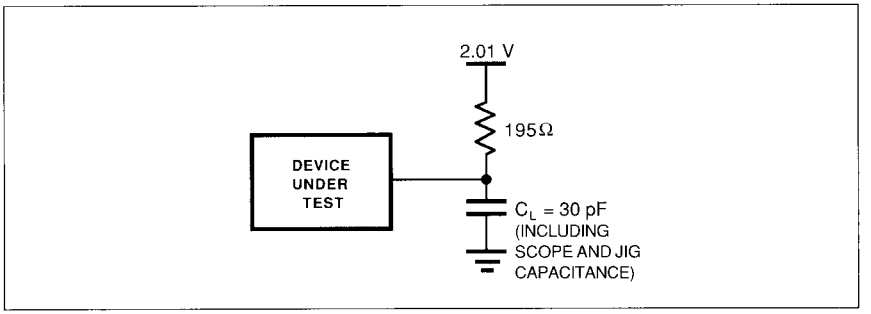


Figure 21. AC Testing Load Circuit



Erasure and Programming

To clear all locations of their programmed contents, expose the device to ultra-violet light source. A dosage of 15 W second/cm^2 is required. This dosage can be obtained with exposure to a wavelength of 2537 Å and intensity of 12000 μW/cm^2 for 15 to 20 minutes. The device should be about 1 inch from the source, and all filters should be removed from the UV light source prior to erasure.

The PSD311 and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although the erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight eventually erases the device. For maximum system reliability, these sources should be avoided. If used in such an environment, the package windows should be covered by an opaque substance.

Upon delivery from WSI, or after each erasure, the PSD311 device has all bits in the PAD and EPROM in the "1" or high state. The configuration bits are in the "0" or low state. The code, configuration, and PAD MAP data are loaded through the procedure of programming

Information for programming the device is available directly from WSI. Please contact your local sales representative.

Pin Assignments

Name	44-Pin PLDCC/ CLDCC Package	44-Pin CPGA Package	52-Pin PQFP Package
$\overline{PSEN}$	1	A_5	46
$\overline{WR}/V_{PP}$ or R/$\overline{W}$	2	A_4	47
RESET	3	B_4	48
PB7	4	A_3	49
PB6	5	B_3	50
PB5	6	A_2	51
PB4	7	B_2	2
PB3	8	B_1	3
PB2	9	C_2	4
PB1	10	C_1	5
PB0	11	D_2	6
GND	12	D_1	7
ALE or AS	13	E_1	8
PA7	14	E_2	9
PA6	15	F_1	10
PA5	16	F_2	11
PA4	17	G_1	12
PA3	18	G_2	15
PA2	19	H_2	16
PA1	20	G_3	17
PA0	21	H_3	18
$\overline{RD}$/E	22	G_4	19
AD0/A0	23	H_4	20
AD1/A1	24	H_5	21
AD2/A2	25	G_5	22
AD3/A3	26	H_6	23
AD4/A4	27	G_6	24
AD5/A5	28	H_7	25
AD6/A6	29	G_7	28
AD7/A7	30	G_8	29
A8	31	F_7	30
A9	32	F_8	31
A10	33	E_7	32
GND	34	E_8	33
A11	35	D_8	34
A12	36	D_7	35
A13	37	C_8	36
A14	38	C_7	37
A15	39	B_8	38
PC0	40	B_7	41
PC1	41	A_7	42
PC2	42	B_6	43
A19/$\overline{CSI}$	43	A_6	44
V_{CC}	44	B_5	45

NOTE: 36. Pins 1, 13, 14, 26, 27, 39, 40, and 52 are No Connect.

Package Information

Figure 22 Drawing L4 — 44 Pin Ceramic Leaded Chip Carrier (CLDCC) with Window (Package Type L)

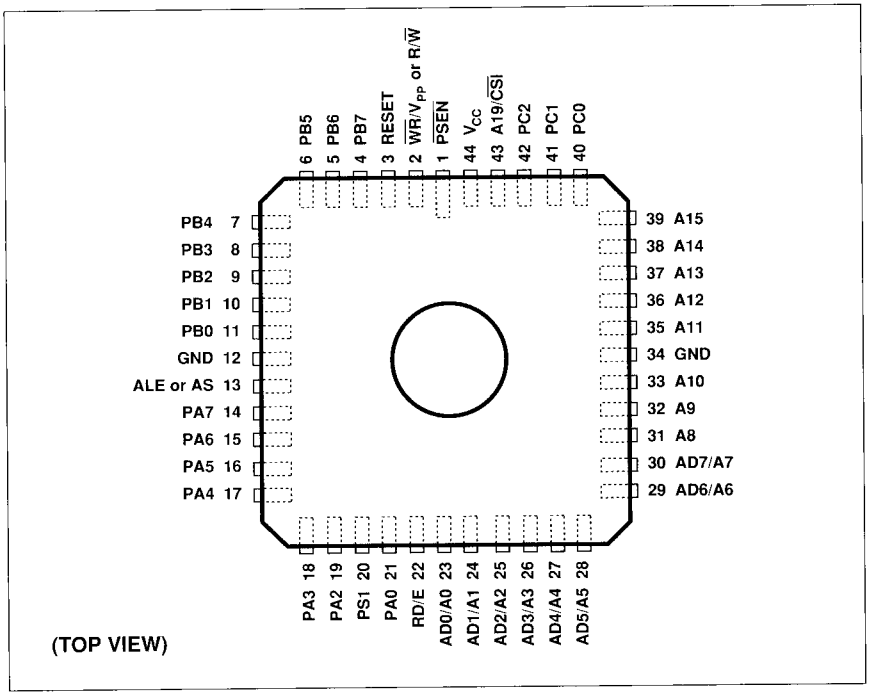


Figure 23. Drawing J2 — 44-Pin Plastic Leaded Chip Carrier (PLDCC) (Package Type J)

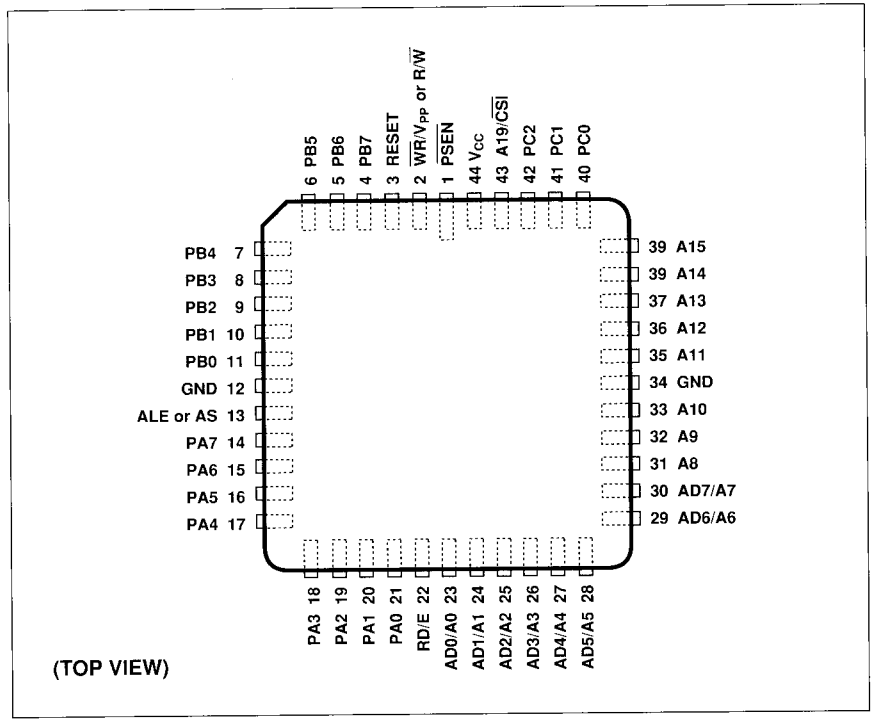


Figure 24. Drawing Q2 — 52-Pin PQFP (Package Type Q)

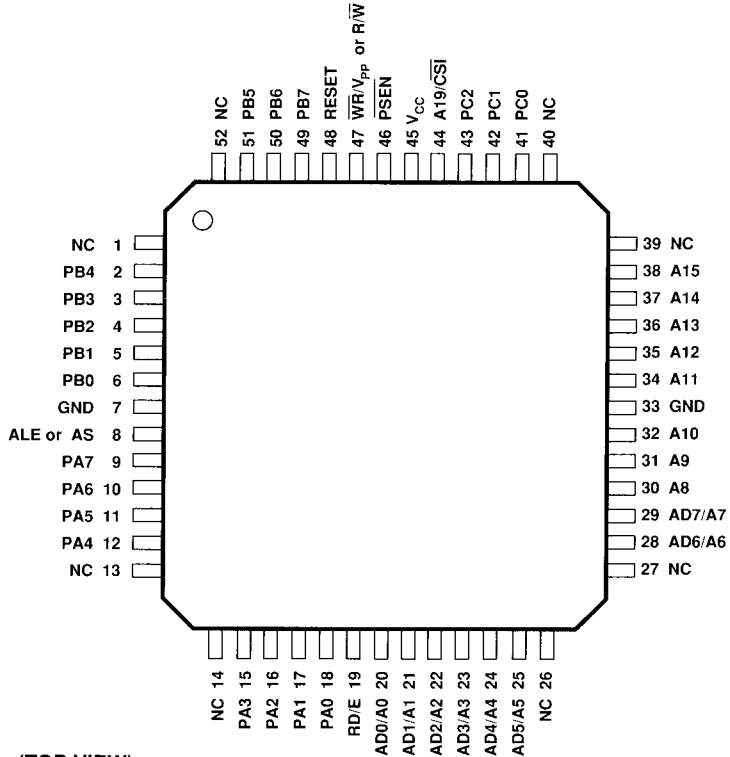
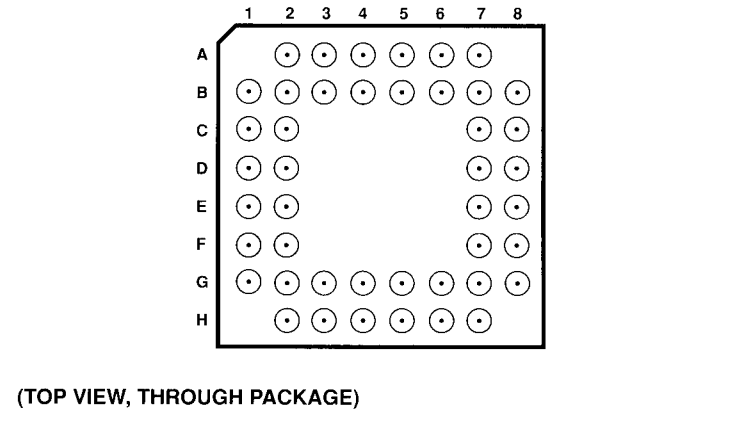


Figure 25. Drawing X2 — 44-Pin CPGA (Package Type X)



Ordering Information

Part Number	Spd. (ns)	Package Type	Package Drawing	Operating Temperature Range	WSI Manufacturing Procedure
PSD311-12J	120	44-pin PLDCC	J2	Commercial	Standard
PSD311-12L	120	44-pin CLDCC	L4	Commercial	Standard
PSD311-12Q	120	52-pin PQFP	Q2	Commercial	Standard
PSD311-12X	120	44-pin CPGA	X2	Commercial	Standard
PSD311-15J	150	44-pin PLDCC	J2	Commercial	Standard
PSD311-15JI	150	44-pin PLDCC	J2	Industrial	Standard
PSD311-15L	150	44-pin CLDCC	L4	Commercial	Standard
PSD311-15LI	150	44-pin CLDCC	L4	Industrial	Standard
PSD311-15LM	150	44-pin CLDCC	L4	Military	Standard
PSD311-15LMB	150	44-pin CLDCC	L4	Military	MIL-STD-883C
PSD311-15Q	150	52-pin PQFP	Q2	Commercial	Standard
PSD311-15X	150	44-pin CPGA	X2	Commercial	Standard
PSD311-15XI	150	44-pin CPGA	X2	Industrial	Standard
PSD311-15XM	150	44-pin CPGA	X2	Military	Standard
PSD311-15XMB	150	44-pin CPGA	X2	Military	MIL-STD-883C
PSD311-20J	200	44-pin PLDCC	J2	Commercial	Standard
PSD311-20JI	200	44-pin PLDCC	J2	Industrail	Standard
PSD311-20L	200	44-pin CLDCC	L4	Commercial	Standard
PSD311-20LI	200	44-pin CLDCC	L4	Industrial	Standard
PSD311-20LM	200	44-pin CLDCC	L4	Military	Standard
PSD311-20LMB	200	44-pin CLDCC	L4	Military	MIL-STD-883C
PSD311-20Q	200	52-pin PQFP	Q2	Commercial	Standard
PSD311-20X	200	44-pin CPGA	X2	Commercial	Standard
PSD311-20XI	200	44-pin CPGA	X2	Industrial	Standard
PSD311-20XM	200	44-pin CPGA	X2	Military	Standard
PSD311-20XMB	200	44-pin CPGA	X2	Military	MIL-STD-883C

PSD311
System Development Tools

System Development Tools

The PSD311 features a complete set of System Development Tools. These tools provide an integrated, easy-to-use software and hardware environment to support PSD311 device development. To run these tools requires an IBM-XT, -AT, or compatible computer, MS-DOS 3.1 or higher, 640K byte RAM, and a hard disk.

Hardware

The PSD311 System Programming Hardware consists of:

- ❑ WS6000 MagicPro Memory and PSD Programmer
- ❑ WS6020 52-pin PSD311 PQFP Package Adaptor
- ❑ WS6021 44-pin LCC Package Adaptor (for CLDCC and PLDCC packages)
- ❑ WS6022 44-pin CPGA Package Adaptor

The MagicPro Programmer is the common hardware platform for programming all WSI programmable products. It consists of an IBM-PC plug-in programmer board and a remote socket adaptor.

Software

The PSD311 System Development Software consists of:

- ❑ WISPER, WSI's Software Environment
- ❑ MAPLE, the PSD311 Location Editor Software
- ❑ MAPPRO, the Device Programming Software

The configuration of the PSD311 device is entered using MAPLE software. MAPPRO software uses the MagicPro programmer and the socket adaptor to configure the PSD311 device, which then can be used in the target system. The development cycle is depicted in Figure 26.

Support

WSI provides a complete set of quality support services to registered System Development Tools owners, including:

- ❑ 12-month software updates
- ❑ Design assistance from WSI field application engineers and group experts
- ❑ 24-hour Electronic Bulletin Board for design assistance via dial-up modem.

Training

WSI provides in-depth, hands-on workshops for the PSD311 device and System Development Tools. Workshop participants learn how to program high-performance, programmable peripherals. Workshops are held at the WSI facility in Fremont, California.

Ordering Information – System Development Tools

PSD-GOLD
- ❑ WISPER Software
- ❑ MAPLE Software
- ❑ User's Manual
- ❑ WSI Support
- ❑ WS6000 MagicPro™ Programmer
- ❑ One Package Adaptor and Two PSD311 Product Samples

PSD-SILVER
- ❑ WISPER Software
- ❑ MAPLE software
- ❑ User's Manual
- ❑ WSI Support

WS6000
- ❑ MagicPro Programmer
- ❑ IBM-PC© Plug-in Adaptor Card
- ❑ Remote Socket Adaptor

WS6020
- ❑ 52-pin PQFP Package Adaptor. Used with the WS6000 MagicPro Programmer

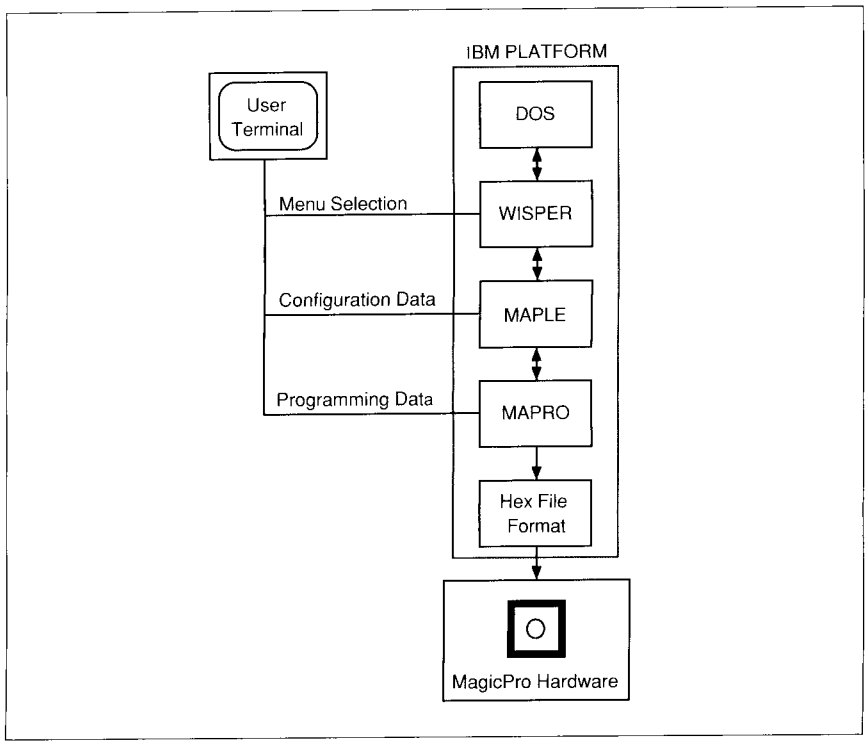
WS6021
- ❑ 44-Pin LCC Package Adaptor for CLDCC and PLDCC Packages. Used with the WS6000 MagicPro Programmer.

WS6022
- ❑ 44-Pin CPGA Package Adaptor. Used with the WS6000 MagicPro Programmer.

WSI Support
Support services include:
- ❑ 12-month Software Update Service
- ❑ Hotline to WSI Application Experts
- ❑ 24-hour access to WSI Electronic Bulletin Board

WSI Training
- ❑ Workshops at WSI, Fremont, CA
- ❑ For details and scheduling, call PSD Marketing (510) 656-5400.

Figure 26. PSD311 Development Cycle



Programmable Peripheral

PSD302

Programmable Microcontroller Peripheral with Memory

Preliminary

Key Features

- ❑ Single Chip Programmable Peripheral for Microcontroller-based Applications
- ❑ 19 Individually Configurable I/O pins that can be used as
  - — Microcontroller I/O port expansion
  - — Programmable Address Decoder (PAD) I/O
  - — Latched address output
  - — Open drain or CMOS
- ❑ Two Programmable Arrays (PAD A & PAD B)
  - — Total of 40 Product Terms and up to 16 Inputs and 24 Outputs
  - — Direct Address Decoding up to 1 Meg address space and up to 16 Meg with paging
  - — Logic replacement
- ❑ "No Glue" Microcontroller Chip-Set
  - — Built-in address latches for multiplexed address/data bus
  - — Non-multiplexed address/data bus mode
  - — Selectable 8 or 16 bit data bus width
  - — ALE and Reset polarity programmable
  - — Selectable modes for read and write control bus as $\overline{RD}/\overline{WR}$, R/$\overline{W}$/E, or R/$\overline{W}$/$\overline{DS}$
  - — BHE/ pin for byte select in 16-bit mode
  - — PSEN/ pin for 8051 users
- ❑ Built-In Page Logic
  - — To Expand the Address Space of Microcontrollers with Limited Address Space Capabilities
  - — Up to 16 pages
- ❑ 512 Kbits of UV EPROM
  - — Configurable as 64K x 8 or as 32K x 16
  - — Divides into 8 equal mappable blocks for optimized mapping
  - — Block resolution is 8K x 8 or 4K x 16
  - — 120 ns EPROM access time, including input latches and PAD address decoding.
- ❑ 16 Kbit Static RAM
  - — Configurable as 2K x 8 or as 1K x 16
  - — 120 ns SRAM access time, including input latches and PAD address decoding
- ❑ Address/Data Track Mode
  - — Enables easy Interface to Shared Resources (Mail Box SRAM) with other Microcontrollers or a Host Processor
- ❑ Built-In Security
  - — Locks the PSD302 Configuration and PAD Decoding
- ❑ Available in a Variety of Packaging
  - — 44 Pin PLDCC and CLDCC
  - — 52 Pin PQFP
  - — 44 Pin CPGA
- ❑ Simple Menu-Driven Software: Configure the PSD302 on an IBM PC
- ❑ Downward Pin and Functionally Compatible with the PSD301

Partial Listing of Microcontrollers Supported

- ❑ **Motorola family:** M6805, M68HC11, M68HC16, M68000/10/20, M60008, M683XX
- ❑ **Intel family:** 8031/8051, 8096/8098, 80186/88, 80196/98
- ❑ **Signetics:** SC80C451, SC80C552
- ❑ **Zilog:** Z8, Z80, Z180
- ❑ **National:** HPC16000

Applications

- ❑ Computers (Workstations and PCs)
  - — Fixed Disk Control, Modem, Imaging, Laser Printer Control
- ❑ Telecommunications
  - — Modem, Cellular Phone, Digital PBX, Digital Speech, FAX, Digital Signal Processing
- ❑ Industrial
  - — Robotics, Power Line Access, Power Line Motor
- ❑ Medical Instrumentation
  - — Hearing Aids, Monitoring Equipment, Diagnostic Tools
- ❑ Military
  - — Missile Guidance, Radar, Sonar, Secure Communications, RF Modems

Introduction

The PSD302 is the latest member in the rapidly growing family of PSD devices. The PSD302 is ideal for microcontroller-based applications, where fast time-to-market, small form factor, and low power consumptions are essential. When combined in an 8- or 16-bit system, virtually any microcontroller (68HC11, 8051, 8096, 16000, etc.) and the PSD302 work together to create a very powerful chip-set solution. This implementation provides all the required control and peripheral elements of a microcontroller-based system peripheral with no external discrete "glue" logic required.

The solution comes complete with simple system software development tools for integrating the PSD302 with the microcontroller. Hosted on the IBM PC platforms or compatibles, the easy to use software enables the designer complete freedom in designing the system.

Product Description

The PSD302 integrates high performance user-configurable blocks of EPROM, SRAM, and programmable logic technology to provide a single chip microcontroller interface. The major functional blocks include two programmable logic arrays, PAD A and PAD B, 512K bits of EPROM, 16K bits of SRAM, input latches, and output ports. The PSD302 is ideal for applications requiring high performance, low power, and very small form factors. These include fixed disk control, modem, cellular telephone, instrumentation, computer peripherals, military and similar applications.

The PSD302 offers a unique single-chip solution for microcontrollers that need:

- ❑ I/O reconstruction (microcontrollers lose at least two I/O ports when accessing external resources).
- ❑ More EPROM and SRAM than the microcontroller's internal memory.
- ❑ Chip-select, control, or latched address lines that are otherwise implemented discretely.
- ❑ An interface to shared external resources.
- ❑ Expanding address space of microcontrollers

WSI's PSD302 (shown in Figure 1) can efficiently interface with, and enhance, any 8- or 16-bit microcontroller system. This is the first solution that provides microcontrollers with port expansion, latched addresses, page logic, two programmable logic arrays PAD A and PAD B, an interface to shared resources, 512K bit EPROM, and 16K bit SRAM on a single chip. The PSD302 does not require any glue logic for interfacing to any 8- or 16-bit microcontroller.

The 8051 microcontroller family can take full advantage of the PSD302's separate program and data address spaces. Users of the 68HCXX family of microcontrollers can change the functionality of the control signals and directly connect the R/$\overline{W}$ and E, or the R/$\overline{W}$ and $\overline{DS}$ signals. Users of 16-bit microcontrollers (including the 80186, 8096, 80196, 16XXX) can use the PSD302 in a 16-bit configuration. Address and data buses can be configured to be separate or multiplexed, whichever is required by the host processor.

Product Discription (Cont.)

The flexibility of the PSD302 I/O ports permits interfacing to shared resources. The arbitration can be controlled internally by PAD A outputs. The user can assign the following functions to these ports: standard I/O pins, chip-select outputs from the PAD A and PAD B, or latched address or multiplexed low-order address/data byte. This enables users to design add-on systems such as disk drives, modems, etc., that easily interface to the host bus (e.g., IBM PC, SCSI).

The PSD302 on-chip programmable address decoder (PAD A) enables the user to map the I/O ports, eight segments of EPROM (as 8K x 8 or as 4K x 16) and SRAM (as 2K x 8 or as 1K x 16) anywhere in the address space of the microcontroller. PAD B can implement up to 4 sum-of-product expressions based on address inputs and control signals.

The page register extends the accessible address space of certain microcontrollers from 64K to 1 M. There are 16 pages that can serve as base address inputs to the PAD, thereby enlarging the address space of 16 address line processors by a factor of 16.

Figure 1. PSD302 Architecture

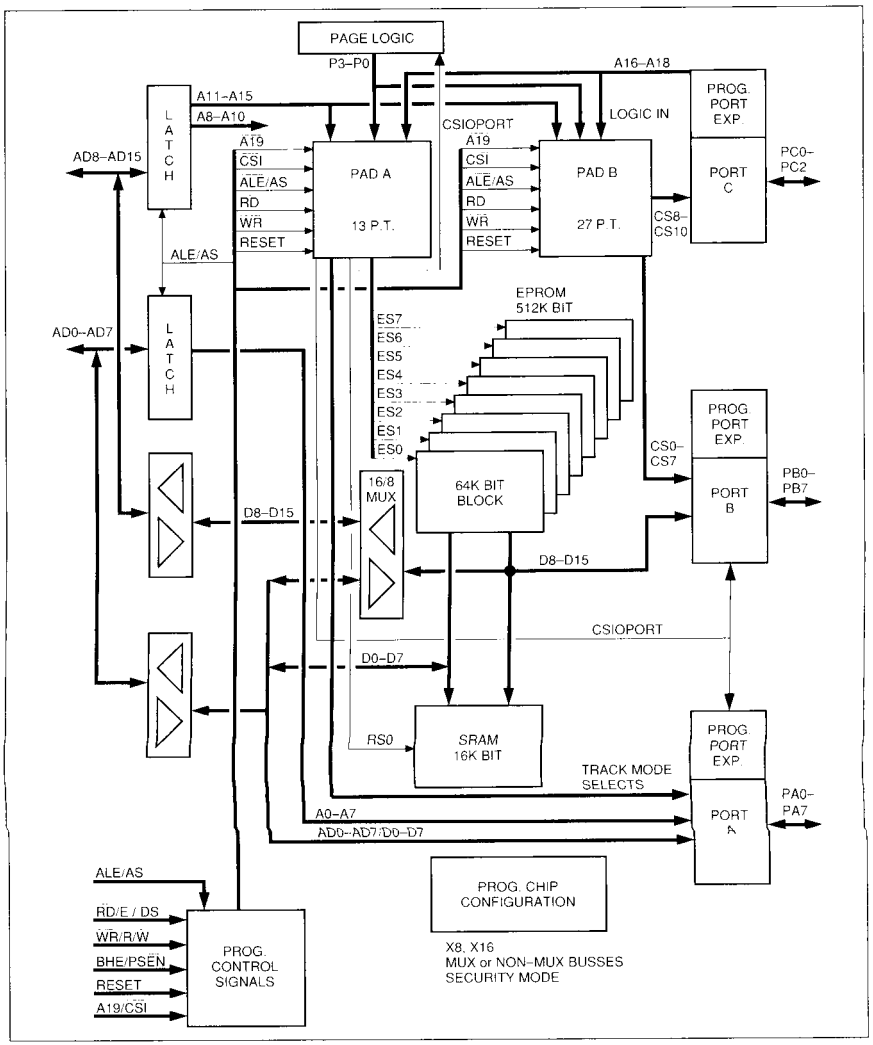


Table 1. PSD302 Pin Descriptions

Name	Type	Description
$\overline{BHE}/\overline{PSEN}$	I	When the data bus width is 8 bits (CDATA = 0), this pin is $\overline{PSEN}$. In this mode, $\overline{PSEN}$ is the active low EPROM read pulse. The SRAM and I/O ports read signal is generated according to the description of the $\overline{WR}/V_{PP}$ or R/$\overline{W}$ and $\overline{RD}/E/\overline{DS}$ pins. If the host processor is a member of the 8031 family, $\overline{PSEN}$ must be connected to the corresponding host pin. In other 8-bit host processors that do not have a special EPROM-only read strobe, PSEN should be tied to V_{CC}. In this case, $\overline{RD}$ or E and R/$\overline{W}$ provide the read strobe for the SRAM, I/O ports, and EPROM. When the data bus width is configured as 16 (CDATA = 1), this pin is $\overline{BHE}$. When $\overline{BHE}$ is low, data bus bits D8–D15 are read from, or written into, the PSD302, depending on the operation being read or write, respectively. In programming mode, this pin is pulsed between V_{PP} and 0.
$\overline{WR}/V_{PP}$ or R/$\overline{W}$	I	In the operating mode, this pin's function is $\overline{WR}$ (CRRWR = 0) or R/$\overline{W}$ (CRRWR = 1) when configured as R/$\overline{W}$. The following tables summarize the read and write operations (CRRWR = 1): CEDS = 0 R/$\overline{W}$ | E | X | 0 | NOP 0 | 1 | write 1 | 1 | read CEDS = 1 R/$\overline{W}$ | $\overline{DS}$ | X | 0 | NOP 0 | 1 | write 1 | 0 | read When configured as $\overline{WR}$, a write operation is executed during an active low pulse. When configured as R/$\overline{W}$, with R/$\overline{W}$ = 1 and E = 1, a read operation is executed; if R/$\overline{W}$ = 0 and E = 1, a write operation is executed. In programming mode, this pin must be tied to V_{PP} voltage.
$\overline{RD}/E/\overline{DS}$	I	The pin function depends on the CRRWR and CEDS configuration bits. If CRRWR = 0, $\overline{RD}$ is an active low read pulse. When CRRWR = 1, this pin and the R/$\overline{W}$ pin define the following cycle type: If CEDS = 0, E is an active high strobe. If CEDS = 1, $\overline{DS}$ is an active low strobe.
$\overline{CSI}$/A19	I	This pin has two configurations. When it is $\overline{CSI}$ (CA19/$\overline{CSI}$ = 0) and the pin is asserted high, the device is deselected and powered down. (See Tables 12 and 13 for the chip state during power-down mode.) If the pin is asserted low, the chip is in normal operational mode. When it is configured as A19, (CA19/$\overline{CSI}$ = 1), this pin can be used as an additional input to the PAD. CADLOG3 = 1 defines the pin as an address; CADLOG3 = 0 defines it as a logic input. If it is an address, A19 can be latched with ALE (CADDHLT = 1) or be a transparent logic input (CADDHLT = 0). In this mode, there is no power-down capability.
RESET	I	This user-programmable pin can be configured to reset on high level (CRESET = 1) or on low level (CRESET = 0). It should remain active for at least 100 ns. See Tables 10 and 11 for the chip state after reset.

Legend: The I/O column abbreviations are: I = input; I/O = input/output; P = power.

NOTE: 1. All the configuration bits mentioned in Table 1 appear in parentheses and are explained in the Configuration Register section.

Table 1. PSD302 Pin Descriptions (Cont.)

Name	Type	Description
ALE or AS	I	In the multiplexed modes, the ALE pin functions as an Address Latch Enable or as an Address strobe and can be configured as an active high or active low signal. The ALE or AS trailing edge latches lines AD15/A15–AD0/A0, A16–A19, and $\overline{BHE}$, depending on the PSD302 configuration. See Table 8. In the non-multiplexed modes, it can be used as a general-purpose logic input to the PAD.
PA7 PA6 PA5 PA4 PA3 PA2 PA1 PA0	I/O	PA7–PA0 is an 8-bit port that can be configured to track AD7/A7–AD0/A0 from the input (CPAF2 = 1). Otherwise (CPAF2 = 0), each bit can be configured separately as an I/O or lower-order latched address line. When configured as an I/O (CPAF1 = 0), the direction of the pin is defined by its direction bit, which resides in the direction register. If a pin is an I/O output, its data bit (which resides in the data register) comes out. When it is configured as a low-order address line (CPAF1 =1), A7–A0 can be made the corresponding output through this port (e.g., PA6 can be configured to be the A6 address line). Each port bit can be a CMOS output (CPACOD = 0) or an open drain output (CPACOD = 1). When the chip is in non-multiplexed mode (CADDRAT = 0), the port becomes the data bus lines (D0–D7). See Figure 4.
PB7 PB6 PB5 PB4 PB3 PB2 PB0	I/O	PB7–PB0 is an 8-bit port for which each bit can be configured as an I/O (CPBF = 1) or chip-select output (CPBF = 0). Each port bit can be a CMOS output (CPBCOD = 0) or an open drain output (CPBCOD = 1). When configured as an I/O, the direction of the pin is defined by its direction bit, which resides in the direction register. If a pin is an I/O output, its data (which resides in the data register) comes out. When configured as a chip-select output, $\overline{CS0}$–$\overline{CS3}$ are a function of up to four product terms of the inputs to the PAD B; $\overline{CS4}$,–$\overline{CS7}$ then are each a function of up to two product terms. When the chip is in non-multiplexed mode (CADDRAT = 0) and the data bus width is 16 (CDATA = 1), the port becomes the data bus (D8–D15). See Figure 6.
PC0 PC1 PC2	I/O	This is a 3-bit port for which each bit is configurable as a PAD A and B input or output. When configured as an input (CPCF = 0), a bit individually becomes an address (CADLOG = 1) or a logic input (CADLOG = 0). The addresses can be latched with ALE (CADDHLT = 1) or be transparent inputs to the PADs (CADDHLT = 0). When a pin is configured as an output (CPCF = 1), it is a function of one product term of all PAD inputs. See Figure 7.
AD0/A0 AD1/A1 AD2/A2 AD3/A3 AD4/A4 AD5/A5 AD6/A6 AD7/A7	I/O	In multiplexed mode, these pins are the multiplexed low-order address/data byte. After ALE latches the addresses, these pins input or output data, depending on the settings of the $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$/V_{PP} or R/$\overline{W}$, and $\overline{BHE}$/$\overline{PSEN}$ pins. In non-multiplexed mode, these pins are the low-order address input.

Table 1. PSD302 Pin Descriptions (Cont.)

Name	Type	Description
AD8/A8 AD9/A9 AD10/A10 AD11/A11 AD12/A12 AD13/A13 AD14/A14 AD15/A15	I/O	In 16-bit multiplexed mode, these pins are the multiplexed high-order address/data byte. After ALE latches the addresses, these pins input or output data, depending on the settings of the $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$/V_{PP} or R/$\overline{W}$, and $\overline{BHE}$/$\overline{PSEN}$ pins. In all other modes, these pins are the high-order address input.
GND	P	V_{SS} (ground) pin.
V_{CC}	P	Supply voltage input.

Operating Modes

The PSD302's four operating modes allow it to interface directly to 8- and 16-bit microcontrollers with multiplexed and non-multiplexed address/data buses. These operating modes are:

- Multiplexed 8-bit address/data bus
- Multiplexed 16-bit address/data bus
- Non-multiplexed address/data, 8-bit data bus
- Non-multiplexed 16-bit address/data bus

Multiplexed 8-bit Address/Data Bus

This mode is used to interface to microcontrollers with an 8-bit data bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is bi-directional and permits the latching of the address when the ALE signal is active. On the same pins, the data is read from or written to the device; this depends on the state of the $\overline{RD}$/E/$\overline{DS}$, $\overline{BHE}$/$\overline{PSEN}$ and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins. The high-order address/data bus (AD8/A8–AD15/A15) contains the high-order address bus byte. Ports A and B can be configured as in Table 2.

Multiplexed 16-bit Address/Data Bus

This mode is used to interface to microcontrollers with a 16-bit data bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is bi-directional and permits the latching of the address when the ALE signal is active. On the same pins, the data is read from or written to the device; this depends on the state of the $\overline{RD}$/E/$\overline{DS}$, $\overline{BHE}$/$\overline{PSEN}$, and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins. The high-order address/data bus (AD8/A8–AD15/A15) is bi-directional and permits latching of the high-order address when the ALE signal is active on the same pins. The high-order data bus is read from or written to the device, depending on the state of the $\overline{RD}$/E/$\overline{DS}$, $\overline{BHE}$/$\overline{PSEN}$, and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins. Ports A and B can be configured as in Table 2.

Non-Multiplexed Address/Data, 8-bit Data Bus

This mode is used to interface to non-multiplexed 8-bit microcontrollers with an 8-bit data bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is the low-order address input bus. The high-order address/data bus (AD8/A8–AD15/A15) is the high-order address bus byte. Port A is the low-order data bus. Port B can be configured as shown in Table 2.

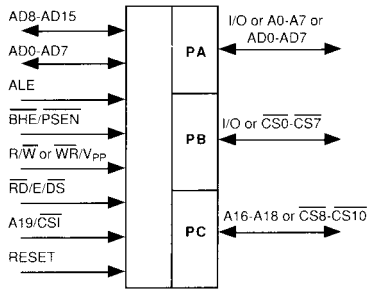
Non-Multiplexed Address/Data, 16-bit Data Bus

This mode is used to interface to non-multiplexed 16-bit microcontrollers with a 16-bit data bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is the low-order address input bus. The high-order address/data bus (AD8/A8–AD15/A15) is the high-order address bus byte. Port A is the low-order data bus. Port B is the high-order data bus.

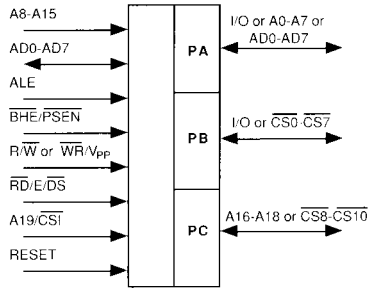
Table 2 summarizes the effect of the different operating modes on ports A, B, and the address/data pins. The configuration of Port C is independent of the four operating modes.

Figure 2. PSD302 Port Configurations

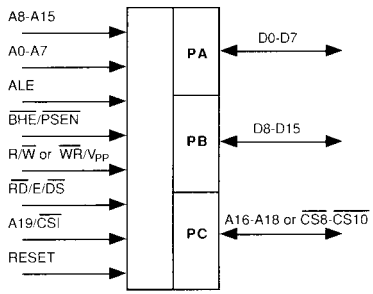
Figure 2 shows the PSDS302's I/O port configurations.



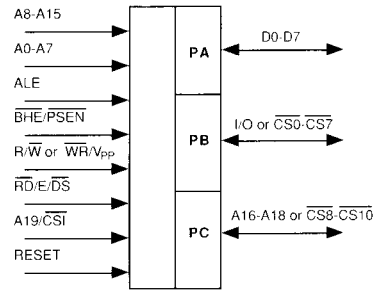
1. PSD302 configured for multiplexed 16-bit address/data bus.



2. PSD302 configured for multiplexed 8-bit address/data bus.



3. PSD302 configured for non-multiplexed 16-bit address/data bus.



4. PSD302 configured for non-multiplexed address/data, 8-bit bus.

Legend: AD8–AD15 = Addresses A8–A15 multiplexed with data lines D8–D15.
AD0–AD7 = Addresses A0–A7 multiplexed with data lines D0–D7.

Table 2. PSD302 Bus and Port Configuration Options

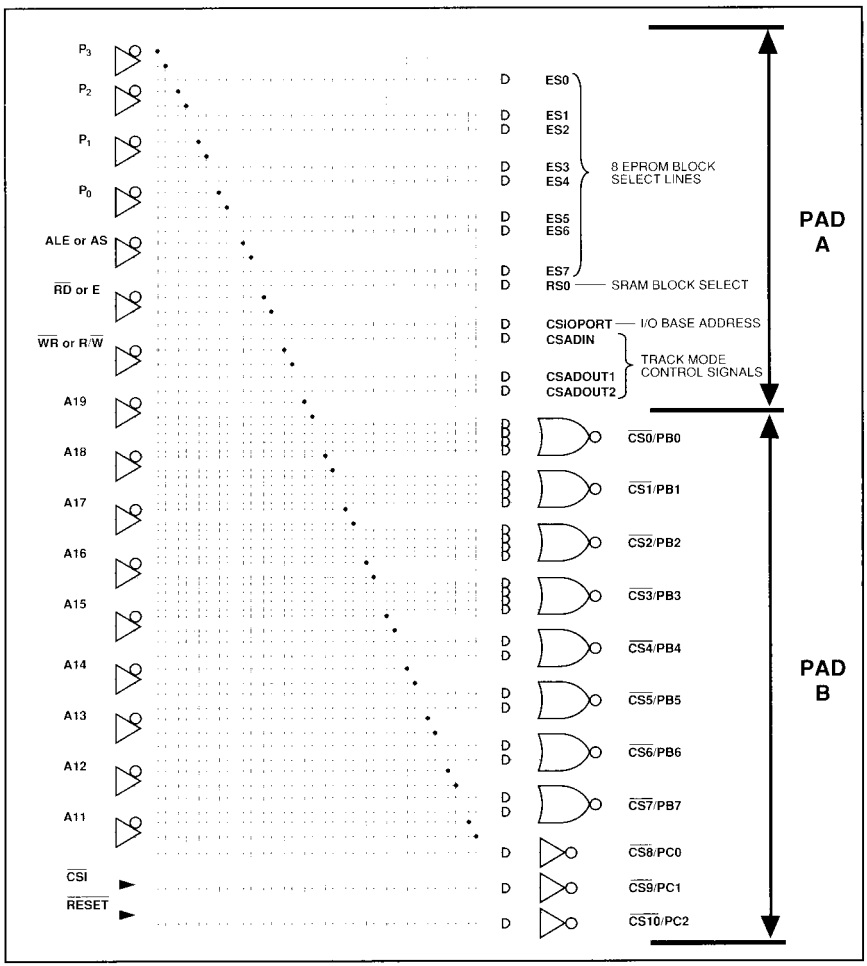
	Multiplexed Address/Data	***Non-Multiplexed Address/Data***
8-bit Data Bus		
Port A	I/O or low-order address lines or Low-order multiplexed address/data byte	D0–D7 data bus byte
Port B	I/O or $\overline{CS0}$–$\overline{CS7}$	I/O and/or $\overline{CS0}$–$\overline{CS7}$
AD0/A0–AD7/A7	Low-order multiplexed address/data byte	Low-order address bus byte
AD8/A8–AD15/A15	High-order multiplexed address data byte	High-order address bus byte
16-bit Data Bus		
Port A	I/O or low-order address lines or Low-order multiplexed address/data byte	Low-order data bus byte
Port B	I/O or $\overline{CS0}$–$\overline{CS7}$	High-order data bus byte
AD0/A0–AD7/A7	Low-order multiplexed address/data byte	Low-order address bus byte
AD8/A8–AD15/A15	High-order multiplexed address/data byte	High-order address bus byte

Programmable Address Decoder (PAD)

The PSD302 consists of two programmable arrays referred to as PAD A and PAD B (Figure 3). PAD A is used to generate chip select signals derived from the input address to the internal EPROM blocks, SRAM, I/O ports, and Track Mode signals. All its I/O functions are listed in Table 3 and shown in Figure 3. PAD B outputs to Ports B and C for off-chip usage.

PAD B can also be used to extend the decoding to select external devices or as a random logic replacement. The input bus to both PAD A and PAD B is the same. Using WSI's MAPLE software, each programmable bit in the PAD's array can have one of three logic states of 0, 1, and don't care (X). In a user's logic design, both PADs can share the same inputs using the X for input signals that are not supposed to affect other functions. The PADs use reprogrammable CMOS EPROM technology and can be programmed and erased by the user.

Figure 3. PSD302 PAD Description



NOTES: 2. $\overline{CSI}$ is a power-down signal. When high, the PAD is in stand-by mode and all its outputs become non-active. See Tables 12 and 13.
3. RESET deselects all PAD output signals. See Tables 10 and 11.
4. A18, A17, and A16 are internally multiplexed with $\overline{CS10}$, $\overline{CS9}$, and $\overline{CS8}$, respectively. Either A18 or $\overline{CS10}$, A17 or $\overline{CS9}$, and A16 or $\overline{CS8}$ can be routed to the external pins of Port C. Port C can be configured as either input or output.

Table 3. PSD302 PAD A and B I/O Functions

	Function
PAD A and PAD B Inputs	
$\overline{CSI}$ or A19	In $\overline{CSI}$ mode (when high), PAD deselects all of its outputs and enters a power-down mode (see Tables 12 and 13). In A19 mode, it is another input to the PAD.
A16–A18	These are general purpose inputs from Port C. See Figure 3, Note 4.
A11–A15	These are address inputs.
P0–P3	These are page number inputs.
$\overline{RD}$ or E	This is the read pulse or enable strobe input.
$\overline{WR}$ or R/$\overline{W}$	This is the write pulse or R/$\overline{W}$ select signal.
ALE	This is the ALE input to the chip.
RESET	This deselects all outputs from the PAD; it can not be used in product term equations. See Tables 10 and 11.
PAD A Outputs	
ES0–ES7	These are internal chip-selects to the 8 EPROM banks. Each bank can be located on any boundary that is a function of one product term of the PAD address inputs.
RS0	This is an internal chip-select to the SRAM. Its base address location is a function of one term of the PAD address inputs.
CSIOPORT	This internal chip-select selects the I/O ports. It can be placed on any boundary that is a function of one product term of the PAD inputs. See Tables 6 and 7.
CSADIN	This internal chip-select, when Port A is configured as a low-order address/data bus in the track mode (CPAF2 = 1), controls the input direction of Port A. CSADIN is gated externally to the PAD by the internal read signal. When CSADIN and a read operation are active, data presented on Port A flows out of AD0/A0–AD7/A7. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 5.
CSADOUT1	This internal chip-select, when Port A is configured as a low-order address/data bus in track mode (CPAF2 = 1), controls the output direction of Port A. CSADOUT1 is gated externally to the PAD by the ALE signal. When CSADOUT1 and the ALE signal are active, the address presented on AD0/A0–AD7/A7 flows out of Port A. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 5.
CSADOUT2	This internal chip-select, when Port A is configured as a low-order address/data bus in the track mode (CPAF2 = 1), controls the output direction of Port A. CSADOUT2 must include the write-cycle control signals as part of its product term. When CSADOUT2 is active, the data presented on AD0/A0–AD7/A7 flows out of Port A. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 5.
PAD B Outputs	
$\overline{CS0}$–$\overline{CS3}$	These chip-select outputs can be routed through Port B. Each of them is a function of up to four product terms of the PAD inputs.
$\overline{CS4}$–$\overline{CS7}$	These chip-select outputs can be routed through Port B. Each of them is a function of up to two product terms of the PAD inputs.
$\overline{CS8}$–$\overline{CS10}$	These chip-select outputs can be routed through Port C. See Figure 3, Note 4. Each of them is a function of one product term of the PAD inputs.

Configuration Bits

The configuration bits shown in Table 4 are non-volatile cells that let the user set the device, I/O, and control functions to the proper operational mode. Table 5 lists all configuration bits. The configuration bits are programmed and verified during the programming phase. In operational mode, they are not accessible. To simplify implementing a specific mode, use the WSI's PSD302 MAPLE software to set the bits.

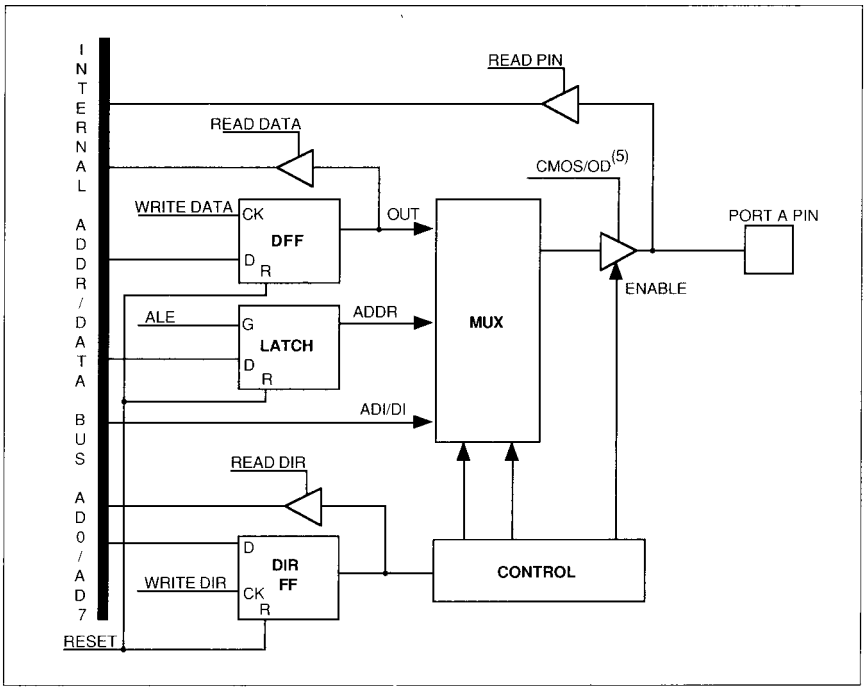
Table 4. PSD302 Non-Volatile Configuration Bits

Use This Bit	To
CDATA	Set the data bus width to 8 or 16 bits.
CADDRDAT	Set the address/data buses to multiplexed or non-multiplexed mode.
CEDS	Determine the polarity and functionality of read and write.
CA19/$\overline{CSI}$	Set A19/$\overline{CSI}$ to $\overline{CSI}$ (power-down) or A19 input.
CALE	Set the ALE polarity.
CPAF2	Set Port A either to track the low-order byte of the address/data multiplexed bus or to select the I/O or address option.
CSECURITY	Set the security on or off (a secured part can not be duplicated).
CRESET	Set the $\overline{RESET}$ polarity.
COMB/SEP	Set $\overline{PSEN}$ and $\overline{RD}$ for combined or separate address spaces (see Figures 8 and 9).
CPAF1 (8 Bits)	Configure each pin of Port A in multiplexed mode to be an I/O or address out.
CPACOD (8 Bits)	Configure each pin of Port A as an open drain or active CMOS pull-up output.
CPBF (8 Bits)	Configure each pin of Port B as an I/O or a chip-select output
CPBCOD (8 Bits)	Configure each pin of Port B as an open drain or active CMOS pull-up output.
CPCF (3 Bits)	Configure each pin of Port C as an address input or a chip-select output.
CADDHLT	Configure pins A16–A19 to go through a latch or to have their latch transparent.
CADLOG (4 Bits)	Configure A16–A19 individually as logic or address inputs.
CLOT	Determine in non-multiplexed mode if address inputs are transparent or latched.
CRRWR	Configure the polarity and control methods of read and write cycles.

Port Functions

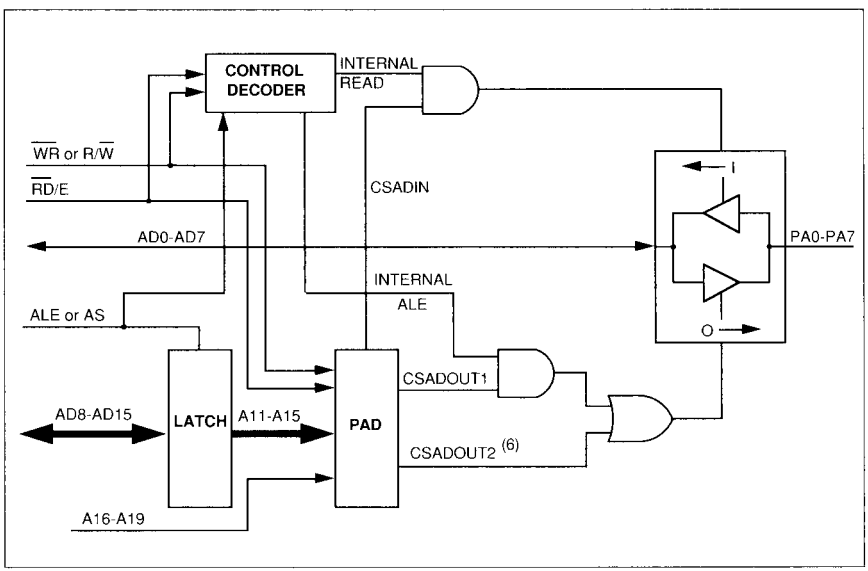
The PSD302 has three I/O ports (Ports A, B, and C) that are configurable at the bit level. This permits great flexibility and a high degree of customization for specific applications. The following is a description of each port. Figure 4 shows the pin structure of Port A.

Figure 4. Port A Pin Structure



NOTE: 5. CMOS/OD determines whether the output is open drain or CMOS.

Figure 5. Port A Track Mode



NOTE: 6. The expression for CSADOUT2 must include the following write operation cycle signals:
For CRRWR = 0, CSADOUT2 must include $\overline{WR}$ = 0.
For CRRWR = 1, CSADOUT2 must include E = 1 and R/$\overline{W}$ = 0.

Table 5. PSD302 Configuration Bits[7,8]

Configuration Bits	No. of Bits	Function
CDATA	1	8-bit or 16-bit Data Bus Width CDATA = 0 eight bits CDATA = 1 sixteen bits
CADDRDAT	1	ADDRESS/DATA Multiplexed (separate buses) CADDRDAT = 0, non-multiplexed CADDRDAT = 1, multiplexed
CA19/$\overline{CSI}$	1	A19 or $\overline{CSI}$ CA19/$\overline{CSI}$ = 0, enable power-down CA19/$\overline{CSI}$ = 1, enable A19 input to PAD
CALE	1	Active HIGH or Active LOW CALE = 0, Active high CALE = 1, Active low
CRESET	1	Active HIGH or Active LOW CRESET = 0, Active low RESET CRESET = 1, Active high RESET
$\overline{COMB}$/SEP	1	Combined or Separate Address Space for SRAM and EPROM 0 = Combined, 1 = Separate
CPAF2	1	Port A AD0–AD7 (address/data multiplexed bus) CPAF2 = 0, address or I/O on Port A (according to CPAF1) CPAF2 = 1, address/data multiplexed on Port A (track mode)
CADDHLT	1	A16–A19 Transparent or Latched CADDHLT = 0, Address latch transparent CADDHLT = 1, Address latched (ALE dependent)
CSECURITY	1	SECURITY On/Off CSECURITY = 0, off CSECURITY = 1, on
CLOT	1	A0–A15 Address Inputs are transparent or ALE-dependent in non-multiplexed modes CLOT = 0, transparent CLOT = 1, ALE-dependent
CRRWR CEDS	2	Determine the polarity and control methods of read and write cycles. CEDS CRRWR 0 0 $\overline{RD}$ and $\overline{WR}$ active low pulses 0 1 R/$\overline{W}$ status and high E pulse 1 1 R/$\overline{W}$ status and low $\overline{DS}$ pulse
CPAF1	8	Port A I/O or A0–A7 CPAF1 = 0, Port A pin is I/O CPAF1 = 1, Port A pin is Ai ($0 \le i \le 7$)
CPACOD	8	Port A CMOS or Open Drain Output CPACOD = 0, CMOS output CPACOD = 1, open-drain output
CPBF	8	Port B is I/O or $\overline{CS0}$– $\overline{CS7}$ CPBF = 0, Port B pin is $\overline{CSI}$ ($0 \le i \le 7$) CPBF = 1, Port B pin is I/O

Table 5. PSD302 Configuration Bits (Cont.)

Configuration Bits	No. of Bits	Function
CPBCOD	8	Port B CMOS or Open Drain CPBCOD = 0, CMOS output CPBCOD = 1, open-drain output
CPCF	3	Port C A16–A18 or $\overline{CS8}$–$\overline{CS10}$ CPCF = 0, Port C pin is Ai (16 ≤ i ≤ 18) CPCF = 1, Port C pin is $\overline{CSi}$ (8 ≤ i ≤ 10)
CADLOG	4	A16–A19 Address or Logic Input CADLOG = 0, Port C pin or A19/$\overline{CSi}$ is logic input CADLOG = 1, Port C pin or A19/$\overline{CSi}$ is Ai (16 ≤ i ≤ 19)
Total Bits	**51**	

NOTES: 7. WSI's MAPLE software will guide the user to the proper configuration choice.
8. In an unprogrammed or erased part, all configuration bits are 0.

2

Port Functions (Cont.)

Port A in Multiplexed Address/Data Mode

The default configuration of Port A is I/O. In this mode, every pin can be set as an input or output by writing into the respective pin's direction flip flop (DIR FF, in Figure 4). As an output, the pin level can be controlled by writing into the respective pin's data flip flop (DFF, in Figure 4). When DIR FF = 1, the pin is configured as an output. When DIR FF = 0, the pin is configured as an input. The controller can read the DIR FF bits by accessing the READ DIR register; it can read the DFF bits by accessing the READ DATA register. Port A pin levels can be read by accessing the READ PIN register. Individual pins can be configured as CMOS or open drain outputs. Open drain pins require external pull-up resistors. For addressing information, refer to Tables 6 and 7.

Alternatively, each bit of Port A can be configured as a low-order latched address bus bit. The address is provided by the port address latch, which latches the address on the trailing edge of ALE. PA0–PA7 can become A0–A7, respectively. This feature of the PSD302 lets the user generate low-order address bits to access external peripherals or memory that require several low-order address lines.

Another mode of Port A (CPAF2 = 1) sets the entire port to track the inputs AD0/A0–AD7/A7, depending on specific address ranges defined by the PAD's CSADIN, CSADOUT1, and CSADOUT2 signals. This feature lets the user interface the microcontroller to shared external resources without requiring external buffers and decoders. In this mode, the port is effectively a bi-directional buffer. The direction is controlled by using the input signals ALE, $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$/V_{PP} or R/$\overline{W}$, and the internal PAD outputs CSADOUT1, CSADOUT2 and CSADIN (see Figure 5). When CSADOUT1 and ALE are true, the address on the input AD0/A7–AD7/A7 pins flows out through Port A. (Carefully check the generation of CSADOUT1, and ensure that it is stable during the ALE pulse; see Figures 22 and 23). When CSADOUT2 is active, a write operation is performed (see note to Figure 5). The data on the input AD0/A7–AD7/A7 pins flows out through Port A. When CSADIN and a read operation is performed (depending on the mode of the $\overline{RD}$/E/$\overline{DS}$ and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins), the data on Port A flows out through the AD0/A7–AD7/A7 pins. In this operational mode, Port A is tri-stated when none of the above-mentioned three conditions exist.

Port Functions (Cont.)

Port A in Non-Multiplexed Address/Data Mode

In this mode, Port A becomes the low order data bus byte of the chip. When reading an internal PSD302 location, data is presented on Port A pins. When writing to an internal PSD302 location, data present on Port A pins is written to that location.

Port B in Multiplexed Address/Data and in 8-Bit Non-Multiplexed Modes

The default configuration of Port B is I/O. In this mode, every pin can be set as an input or output by writing into the respective pin's direction flip flop (DIR FF, in Figure 6). As an output, the pin level can be controlled by writing into the respective pin's data flip flop (DFF, in Figure 6). When DIR FF = 1, the pin is configured as an output. When DIR FF = 0, the pin is configured as an input. The controller can read the DIR FF bits by accessing the READ DIR register; it can read the DFF bits by accessing the READ DATA register. Port B pin levels can be read by accessing the READ PIN register. Individual pins can be configured as CMOS or open drain outputs. Open drain pins require external pull-up resistors. For addressing information, refer to Tables 6 and 7.

Alternatively, each bit of Port B can be configured to provide a chip-select output signal from PAD B. PB0–PB7 can provide $\overline{CS0}$–$\overline{CS7}$, respectively. Each of the signals $\overline{CS0}$–$\overline{CS3}$ is comprised of four product terms.Thus, up to four ANDed expressions can be ORed while deriving any of these signals. Each of the signals $\overline{CS4}$–$\overline{CS7}$ is comprised of two product terms. Thus, up to two ANDed expressions can be ORed while deriving any of these signals.

Port B in 16-Bit Non-Multiplexed Address/Data Mode

In this mode, Port B becomes the high-order data bus byte of the chip. When reading an internal PSD302 high-order data bus byte location, the data is presented on Port B pins. When writing to an internal PSD302 high-order data bus byte location, data present on Port B is written to that location. See Table 9.

Accessing the I/O Port Registers

Tables 6 and 7 show the offset values with the respect to the base address defined by the CSIOPORT. They let the user access the corresponding registers.

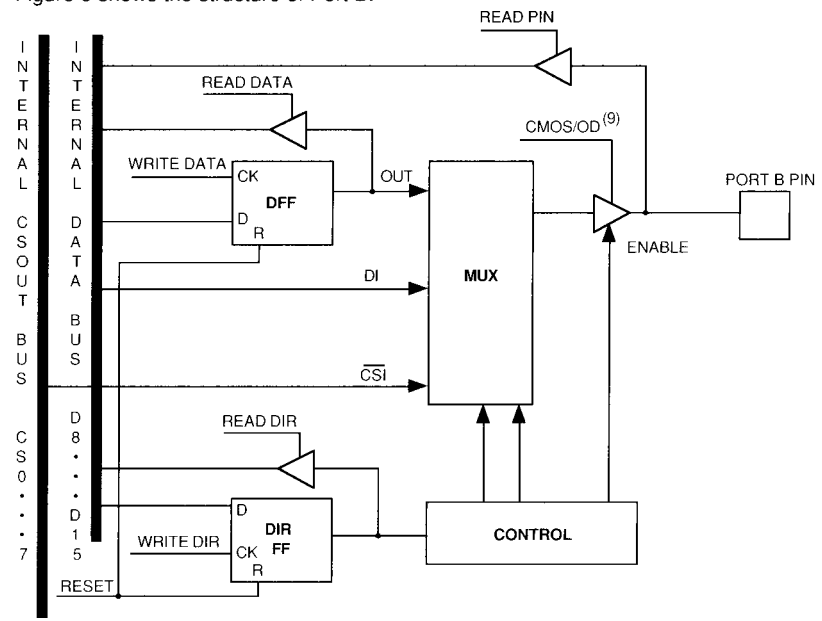
Port C in All Modes

Each pin of Port C (shown in Figure 7) can be configured as an input to PAD A and PAD B or output from PAD B. As inputs, the pins are named A16–A18. Although the pins are given names of the high-order address bus, they can be used for any other address lines or logic inputs to PAD A and PAD B. For example, A8–A10 can also be connected to those pins, improving the boundaries of $\overline{CS0}$–$\overline{CS7}$ resolution to 256 bytes. As inputs, they can be individually configured to be logic or address inputs. A logic input uses the PAD only for Boolean equations that are implemented in any or all of the $\overline{CS0}$–$\overline{CS10}$ PAD B outputs. Port C addresses can be programmed to latch the inputs by the trailing edge ALE or to be transparent.

Alternatively, PC0–PC2 can become $\overline{CS8}$–$\overline{CS10}$ outputs, respectively, providing the user with more external chip-select PAD outputs. Each of the signals $\overline{CS8}$–$\overline{CS10}$ is comprised of one product term.

Figure 6. Port B Pin Structure

Figure 6 shows the structure of Port B.



NOTE: 9. CMOS/OD determines whether the output is open drain or CMOS.

Table 6. I/O Port Addresses in an 8-bit Data Bus Mode

Register Name	Byte Size Access of the I/O Port Registers Offset from the CSIOPORT
Pin Register of Port A	+ 2 (accessible during read operation only)
Direction Register of Port A	+ 4
Data Register of Port A	+ 6
Pin Register of Port B	+ 3 (accessible during read operation only)
Direction Register of Port B	+ 5
Data Register of Port B	+ 7

Table 7. I/O Port Addresses in an 16-bit Data Bus Mode[10,11]

Register Name	Word Size Access of the I/O Port Registers Offset from the CSIOPORT
Pin Register of Ports B and A	+ 2 (accessible during read operation only)
Direction Register of Ports B and A	+ 4
Data Register of Ports B and A	+ 6

NOTES: 10. When the data bus width is 16, Port B registers can only be accessed if the $\overline{BHE}$ signal is low.
11. I/O Ports A and B are still byte-addressable, as shown in Table 6. For I/O Port B register access, $\overline{BHE}$ must be low.

Port Functions (Cont.)

ALE/AS and AD0/A0–AD15/A15 in Non-Multiplexed Modes

In non-multiplexed modes, AD0/A0–AD15/A15 are address inputs only and can become transparent (CLOT = 0) or ALE dependent (CLOT = 1). In transparent mode, the ALE/AS pin can be used as an additional logic input to the PADs. The non-multiplexed ALE dependent mode is useful in applications for which the host processor has a multiplex address/data bus and AD0/A0–AD7/A7 are not multiplexed with A0–A7 but rather are multiplexed with other address lines. In these applications, Port A serves as a data bus and each of its pins can be directly connected to the corresponding host's multiplexed pin, where that data bit is expected. (See Table 8.)

EPROM

The PSD302 has 512K bits of EPROM. Depending on the configuration of the data bus, the EPROM can be organized as 64K x 8 (8-bit data bus) or as 32K x 16 (16-bit data bus). The EPROM has 8 banks of memory. Each bank can be placed in any address location by programming the PAD. Bank0–Bank7 can be selected by PAD outputs ES0–ES7, respectively. The EPROM banks are organized as 8K x 8 (8-bit data bus) or as 4K x 16 (16-bit data bus).

SRAM

The PSD302 has 16K bits of SRAM. Depending on the configuration of the data bus, the SRAM organization can be 2K x 8 (8-bit data bus) or 1K x 16 (16-bit data bus). The SRAM is selected by the RS0 output of the PAD.

Page Register

The page register consists of four flip-flops, which can be read from, or written to, through the I/O address space (CSIOPORT). The page register is connected to the D3–D0 lines. The Page Register address is CSIOPORT + 18H. The page register outputs are P3–P0, which are fed into the PAD. This enables the host microcontroller to enlarge its address space by a factor of 16 (there can be a maximum of 16 pages). See Figure 8.

Control Signals

The PSD302 control signals are $\overline{WR}/V_{PP}$ or R/$\overline{W}$, $\overline{RD}$/E/$\overline{DS}$, ALE, $\overline{BHE}/\overline{PSEN}$, Reset, and A19/$\overline{CSI}$. Each of these signals can be configured to meet the output control signal requirements of various microcontrollers.

$\overline{WR}/V_{PP}$ or R/$\overline{W}$

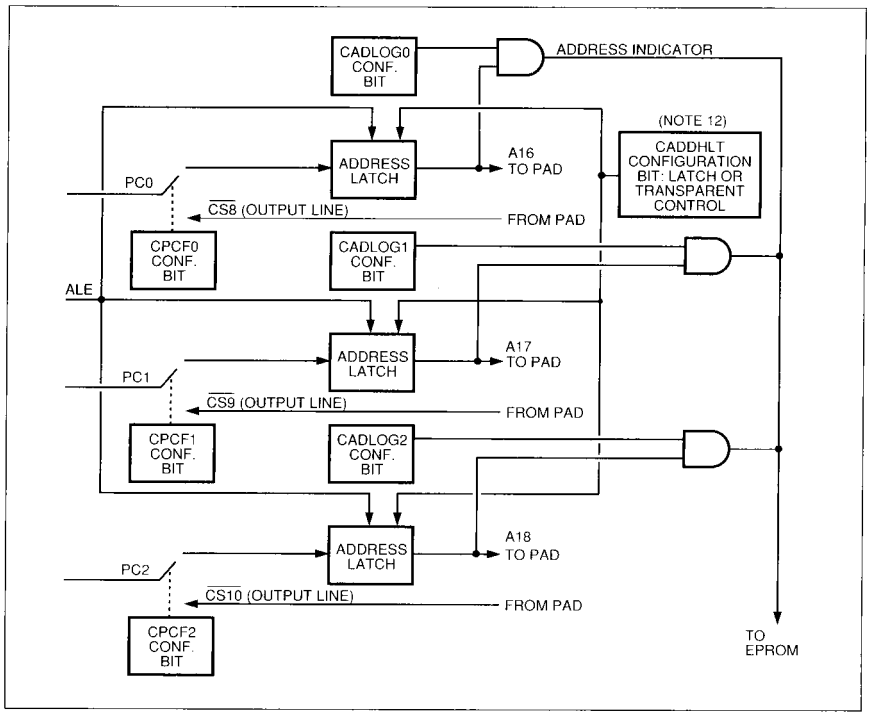
In operational mode, this signal can be configured as $\overline{WR}$ or R/$\overline{W}$. As $\overline{WR}$, all write operations to the PSD302 are activated by an active low signal on this pin. As R/$\overline{W}$, the pin works with the E strobe of the $\overline{RD}$/E/$\overline{DS}$ pin. When R/$\overline{W}$ is high, an active high signal on the $\overline{RD}$/E/$\overline{DS}$ pin performs a read operation. When R/$\overline{W}$ is low, an active high signal on the $\overline{RD}$/E/$\overline{DS}$ pin performs a write operation.

$\overline{RD}$/E/$\overline{DS}$

In operational mode, this signal can be configured as $\overline{RD}$, E, or $\overline{DS}$. As $\overline{RD}$, all read operations to the PSD302 are activated by an active low signal on this pin. As E, the pin works with the R/$\overline{W}$ signal of the $\overline{WR}/V_{PP}$ or R/$\overline{W}$ pin. When R/$\overline{W}$ is high, an active high signal on the $\overline{RD}$/E/$\overline{DS}$ pin performs a read operation. When R/$\overline{W}$ is low, an active high signal on the $\overline{RD}$/E/$\overline{DS}$ pin performs a write operation.

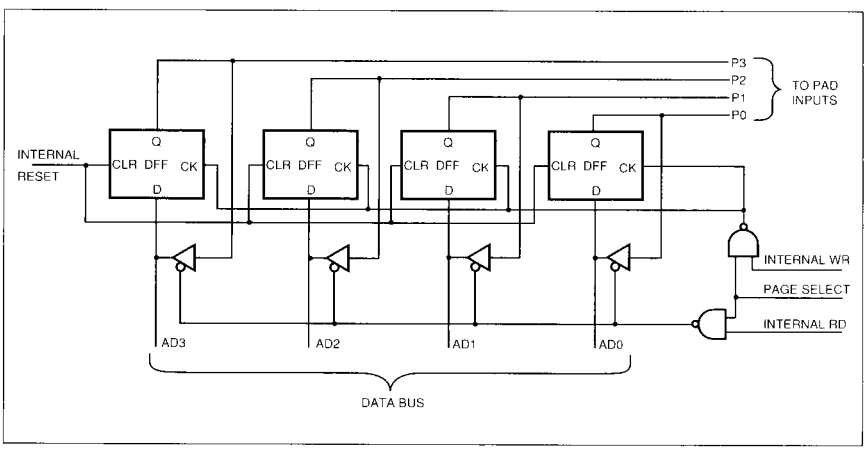
As $\overline{DS}$, the pin functions with the R/$\overline{W}$ signal as an active low data strobe signal. As $\overline{DS}$, the R/$\overline{W}$ defines the mode of operation (Read or Write).

Figure 7. Port C Structure



NOTE: 12. The CADDHLT configuration bit determines if A18–A16 are transparent via the latch, or if they must be latched by the trailing edge of the ALE strobe.

Figure 8. Page Register



Control Signals (Cont.)

ALE or AS

ALE polarity is programmable. When programmed to be active high, a high on the pin causes the input address latches, Port A address latches, Port C, and A19 address latches to be transparent. The falling edge of ALE locks the information into the latches. When ALE is programmed to be active low, a low on the pin causes the input address latches, Port A address latches, Port C, and A19 address latches to be transparent. The rising edge of ALE locks the appropriate information into the latches.

$\overline{BHE}$/$\overline{PSEN}$

This pin's function depends on the PSD302 data bus width. If it is 8, the pin is $\overline{PSEN}$; if it is 16, the pin is $\overline{BHE}$. In 8-bit mode, the $\overline{PSEN}$ function enables the user to work with two address spaces: program memory and data memory (if COMB/SEP = 1). In this mode, an active low signal on the $\overline{PSEN}$ pin causes the EPROM to be read if selected. The SRAM and I/O ports read operation are done by $\overline{RD}$ low (CRRWR = 0), or by E high and R/$\overline{W}$ high (CRRWR = 1, CEDS = 0) or by $\overline{DS}$ low and R/$\overline{W}$ high (CRRWR, CEDS = 1).

Figure 9. Combined Address Space

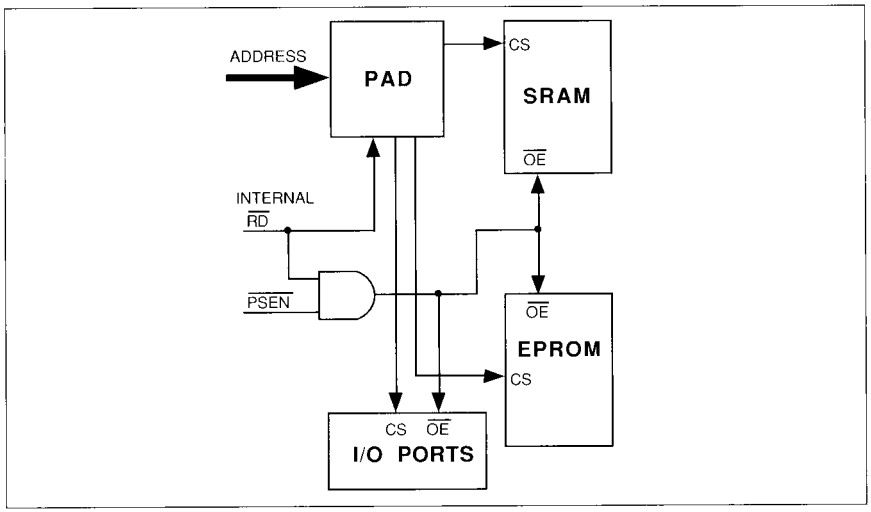
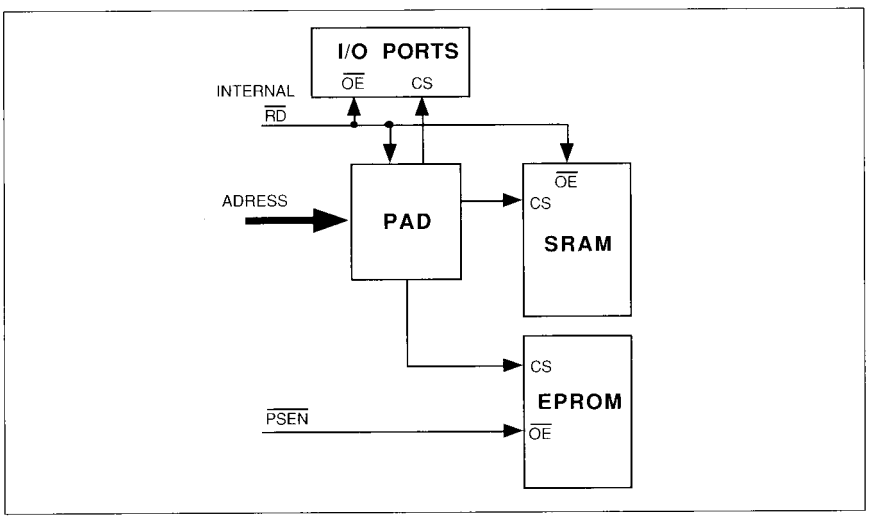


Figure 10. 8031-Type Separate Code and Data Address Spaces



Control Signals (Cont.)

BHE/PSEN

Whenever a member of the 8031 family (or any other similar microcontroller) is used, the PSD302's $\overline{PSEN}$ pin must be connected to the $\overline{PSEN}$ pin of the microcontroller.

If COMB/SEP = 0, the address spaces of the program and the data are combined. In this configuration (except for the 8031-type case mentioned above), the $\overline{PSEN}$ pin must be tied high to V_{CC}, and the EPROM, SRAM, and I/O ports are read by $\overline{RD}$ low (CRRWR = 0), or by E high and R/$\overline{W}$ high (CRRWR = 1, CEDS = 0) or by $\overline{DS}$ low and R/$\overline{W}$ high (CRRWR, CEDS = 1). See Figures 9 and 10.

In $\overline{BHE}$ mode, this pin enables accessing of the upper-half byte of the data bus. A low on this pin enables a write or read operation to be performed on the upper half of the data bus (see Table 9).

Table 8. Signal Latch Status in All Operating Modes

Signal Name	Configuration Bits	Configuration Mode	Signal Latch Status
AD8/A8–AD15/A15	CDATA , CADDRDAT, CLOT = 0	8-bit data, non-multiplexed	Transparent
	CDATA, CADDRDAT = 0, CLOT = 1		ALE Dependent
	CDATA = 1, CADDRDAT, CLOT = 0	16-bit data, non-multiplexed	Transparent
	CDATA = 1, CADDRDAT = 0, CLOT = 1		ALE Dependent
	CDATA = 0, CADDRDAT = 1	8-bit data, multiplexed	Transparent
	CDATA = 1, CADDRDAT = 1	16-bit data, multiplexed	ALE Dependent
AD0/A0-AD7/A7	CADDRDAT = 0, CLOT = 0	non-multiplexed modes	Transparent
	CADDRDAT = 0, CLOT = 1		ALE Dependent
	CADDRDAT = 1	multiplexed modes	ALE Dependent
$\overline{BHE}$/$\overline{PSEN}$	CDATA = 0	8-bit data, $\overline{PSEN}$ is active	Transparent
	CDATA = 1, CADDRDAT = 0	16-bit data, non-multiplexed mode, $\overline{BHE}$ is active	Transparent
A19 and PC2–PC0	CDATA = 1, CADDRDAT = 1	16-bit data, multiplexed mode, $\overline{BHE}$ is active	ALE Dependent
	CADDHLT = 0	A16–A19 can become logic inputs	Transparent
	CADDHLT = 1	A16–A19 can become multiplexed address lines	ALE Dependent

Control Signals (Cont.)

RESET

This is an asynchronous input pin that clears and initializes the PSD302. Reset polarity is programmable (active low or active high). Whenever the PSD302 reset input is driven active for at least 100 ns, the chip is reset. During boot-up (V_{CC} applied), the device is automatically reset internally (internal automatic reset is over by the time V_{CC} operating range has been achieved during boot-up). Tables 10 and 11 indicate the state of the part during and after reset.

A19/$\overline{CSI}$

When configured as $\overline{CSI}$, a high on this pin deselects, and powers down, the chip. A low on this pin puts the chip in normal operational mode. For PSD302 states during the power-down mode, see Tables 12 and 13, and Figure 11.

In A19 mode, the pin is an additional input to the PAD. It can be used as an address line (CADLOG3 = 1) or as a general-purpose logic input (CADLOG3 = 0). A19 can be configured as ALE dependent or as transparent input (see Table 8). In this mode, the chip is always enabled.

Table 9. High/Low Byte Selection Truth Table (in 16-Bit Configuration Only)

$\overline{BHE}$	A_0	Operation
0	0	Whole Word
0	1	Upper Byte From/To Odd Address
1	0	Lower Byte From/To Even Address
1	1	None

Table 10. Signal States During and After Reset

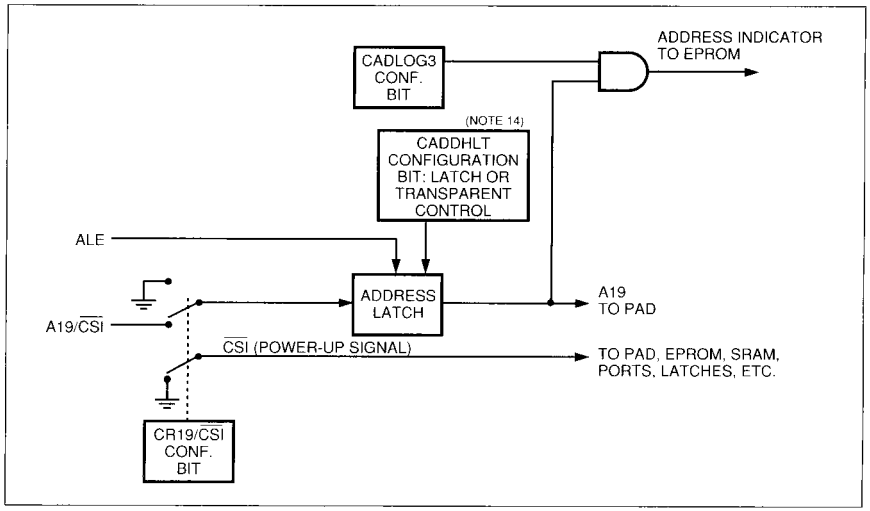
Signal	Configuration Mode	Condition
AD0/A0–AD15/A15	All	Input
PA0–PA7) (Port A	I/O Tracking AD0/A0–AD7 Address outputs A0–A7	Input Input Low
PB0–PB7 (Port B)	I/O $\overline{CS7}$–$\overline{CS0}$ CMOS outputs $\overline{CS7}$–$\overline{CS0}$ open drain outputs	Input High Tri-stated
PC0–PC2 (Port C)	Address inputs A16–A18 $\overline{CS8}$–$\overline{CS10}$ CMOS outputs	Input High

Table 11. Internal States During and After Reset

Component	Signals	Contents
PAD	$\overline{CS0}$–$\overline{CS10}$	All = 1 (Note 13)
	CSADIN, CSADOUT1, CSADOUT2, CSIOPORT, RS0, ES0–ES7	All = 0 (Note 13)
Data register A Direction register A Data register B Direction register B	n/a n/a n/a n/a	0 0 0 0

NOTE: 13. All PAD outputs are in a non-active state.

Figure 11. A19/CSI Cell Structure



NOTES: 14. The CADDHLT configuration bit determines if A19–A16 are transparent via the latch, or if they must be latched by the trailing edge of the ALE strobe.

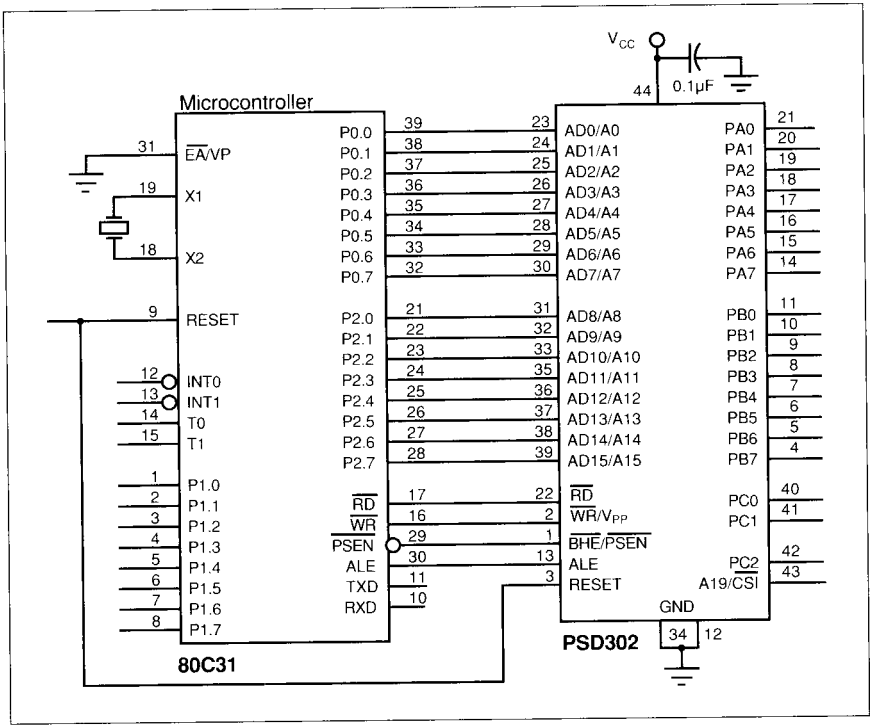
Table 12. Signal States During Power-Down Mode

Signal	Configuration Mode	Condition
AD0/A0–AD15/A15	All	Input
PA0–PA7	I/O Tracking AD0/A0–AD7/A7 Address outputs A0–A7	Unchanged Input All 1's
PB0–PB7	I/O $\overline{CS0}$–$\overline{CS7}$ CMOS outputs $\overline{CS0}$–$\overline{CS7}$ open drain outputs	Unchanged All 1's Tri-stated
PC0–PC2	Address inputs A18–A16 $\overline{CS8}$–$\overline{CS10}$ CMOS outputs	Input All 1's

Table 13. Internal States During Power-Down

Component	Signals	Contents
PAD	$\overline{CS0}$–$\overline{CS10}$	All 1's (deselected)
	CSADIN, CSADOUT1, CSADOUT2, CSIOPORT, RS0, ES0–ES7	All 0's (deselected)
Data register A Direction register A Data register B Direction register B	n/a n/a n/a n/a	All unchanged

Figure 12. PSD302 Interface With Intel's 80C31



The configuration bits for Figure 12 are:

CRESET	1	COMB/SEP	0 or 1 (both valid)
CALE	0	CRRWR	0
CDATA	0	CEDS	0
CADDRDAT	1		

All other configuration bits may vary according to the application requirements.

Security Mode

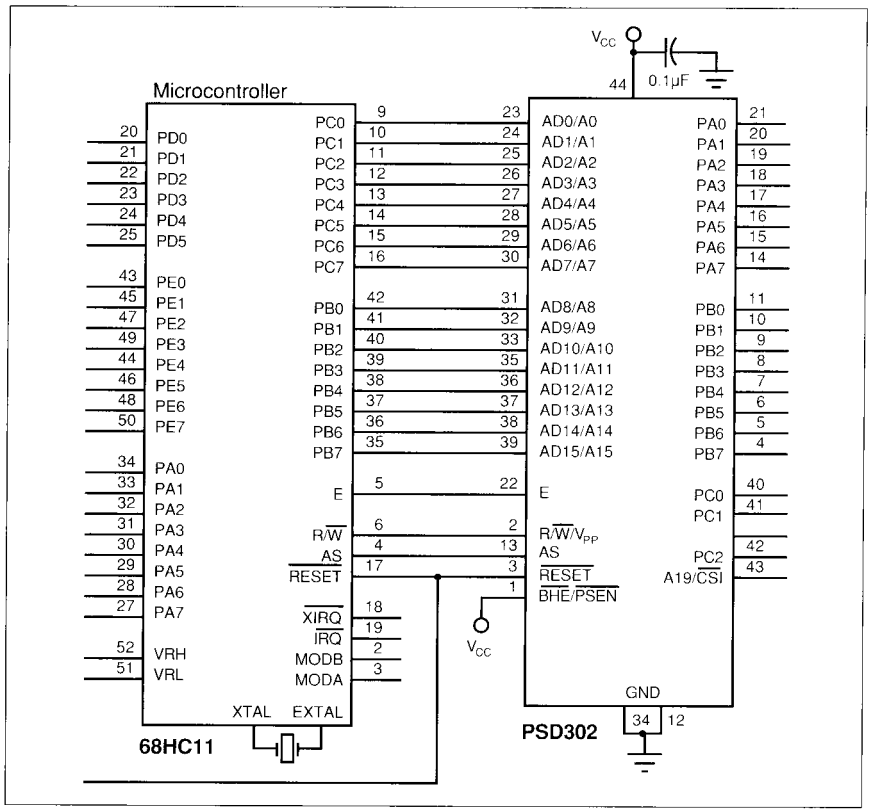
Security Mode in the PSD302 locks the contents of the PAD A , PAD B and all the configuration bits. The EPROM, SRAM, and I/O contents can be accessed only through the PAD. The Security Mode can be set by the MAPLE or Programming software. In window packages, the mode is erasable through UV full part erasure. In the security mode, the PSD302 contents cannot be copied on a programmer.

System Applications

In Figure 12, the PSD302 is configured to interface with Intel's 80C31, which is a 16-bit address/8-bit data bus microcontroller. Its data bus is multiplexed with the low-order address byte. The 80C31 uses signals $\overline{RD}$ to read from data memory and $\overline{PSEN}$ to read from code memory. It uses $\overline{WR}$ to write into the data memory. It also uses active high reset and ALE signals. The rest of the configuration bits as well as the unconnected signals (not shown) are application specific and, thus, user dependent.

In Figure 13, the PSD302 is configured to interface with Motorola's 68HC11, which is a 16-bit address/8-bit data bus microcontroller. Its data bus is multiplexed with the low-order address byte. The 68HC11 uses E and R/$\overline{W}$ signals to derive the read and write strobes. It uses the term AS (address strobe) for the address latch pulse. RESET is an active low signal. The rest of the configuration bits as well as the unconnected signals (not shown) are application specific and, thus, user dependent.

Figure 13. PSD302 Interface With Motorola's 68HC11



The configuration bits for Figure 13 are:

CRESET	0	COMB/SEP	0
CALE	0	CRRWR	1
CDATA	0	CEDS	0
CADDRDAT	1		

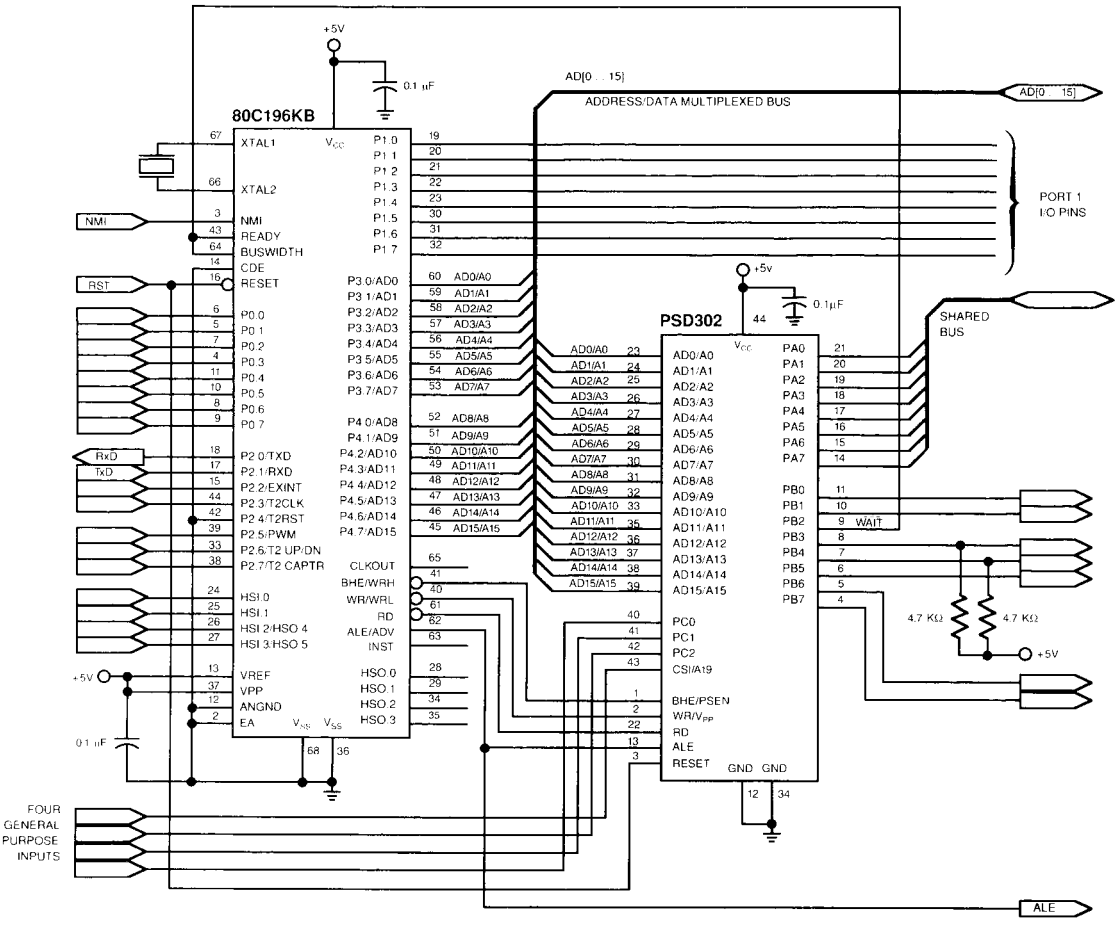
All other configuration bits may vary according to the application requirements.

System Applications (Cont.)

In Figure 14, the PSD302 is configured to work directly with Intel's 80C196KB microcontroller, which is a 16-bit address/16-bit data bus processor. Address and data lines multiplexed. In the example shown, all configuration bits are set. The PSD302 is configured to use PC0, PC1, PC2, and $\overline{CSI}$/A19 as A16, A17, A18, and A19 inputs, respectively. These signals are independent of the ALE pulse (latch-transparent). They are used as four general-purpose logic inputs that take part in the PAD equations implementation.

Port A is configured to work in the special track mode, in which (for certain conditions) PA0–PA7 tracks lines AD0/A0–AD7/A7. Port B is configured to generate $\overline{CS0}$–$\overline{CS7}$. In this example, PB2 serves as a $\overline{WAIT}$ signal that slows down the 80C196KB during the access of external peripherals. These 8-bit wide peripherals are connected to the shared bus of Port A. The $\overline{WAIT}$ signal also drives the buswidth input of the microcontroller, so that every external peripheral cycle becomes an 8-bit data bus cycle. PB3 and PB4 are open-drain output signals; thus, they are pulled up externally.

Figure 14. PSD302 Interface With Intel's 80C196KB.



The configuration bits for Figure 14 are:

CRESET	0	CSECURITY	Don't care
CALE	0	CPCF2, CPCF1, CPCF0	0, 0, 0
CDATA	1	CPACOD7–CPACOD0	00H
CADDRDAT	1	CPBF7–CPBF0	00H
CPAF1	Don't care	CPBCOD7–CPBCOD0	18H
CPAF2	1	CEDS	0
CA19/$\overline{CSI}$	1	CADLOG3—CADLOG0	0H
CRRWR	0		
COMB/SEP	0		
CADDHLT	0		

Absolute Maximum Ratings[15]

Symbol	Parameter	Condition	Min	Max	Unit
T_{STG}	Storage Temperature		– 65	+ 150	°C
	Voltage on any Pin	With Respect to GND	– 0.6	+ 7	V
V_{PP}	Programming Supply Voltage	With Respect to GND	– 0.6	+ 14	V
V_{CC}	Supply Voltage	With Respect to GND	– 0.6	+ 7	V
	ESD Protection			>2000	V

NOTE: 15. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at theses or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Operating Range

Range	Temperature	V_{CC}	Tolerance		
			-12	-15	-20
Commercial	0° C to +70°C	+ 5 V	± 5%	± 10%	± 10%
Industrial	–40° C to +80°C	+ 5 V		± 10%	± 10%
Military	–55° C to +125°C	+ 5 V		± 10%	± 10%

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	-12 Version	4.75	5	5.25	V
V_{CC}	Supply Voltage	-15/-20 Versions	4.5	5	5.5	V
V_{IH}	High-level Input Voltage	V_{CC} = 4.5 V to 5.5 V	2			V
V_{IL}	Low-level Input Voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	V

DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	Output Low Voltage	I_{OL} = 20 µA V_{CC} = 4.5 V		0.01	0.1	V
		I_{OL} = 8 mA V_{CC} = 4.5 V		0.15	0.45	
V_{OH}	Output High Voltage	I_{OH} = –20 µA V_{CC} = 4.5 V	4.4	4.49		V
		I_{OH} = –2 mA V_{CC} = 4.5 V	2.4	3.9		
I_{SB1}	V_{CC} Standby Current (CMOS) (Notes 16 and 18)	Comm'l		50	100	µA
		Ind/Mil		75	150	
I_{SB2}	V_{CC} Standby Current (TTL) (Notes 17 and 18)	Comm'l		1.5	3	mA
		Ind/Mil		2	3.2	
I_{CC1}	Active Current (CMOS) (SRAM Not Selected) (Notes 16 and 19)	Comm'l (Note 20)		16	35	mA
		Comm'l (Note 21)		28	50	
		Ind/Mil (Note 20)		16	45	
		Ind/Mil (Note 21)		28	60	

DC Characteristics (Cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC2}	Active Current (CMOS) (SRAM Block Selected) (Notes 16 and 19)	Comm'l (Note 20)		47	80	mA
		Comm'l (Note 21)		59	95	
		Ind/Mil (Note 20)		47	100	
		Ind/Mil (Note 21)		59	115	
I_{CC3}	Active Current (TTL) (SRAM Not Selected) (Notes 17 and 19)	Comm'l (Note 20)		36	65	mA
		Comm'l (Note 21)		58	80	
		Ind/Mil (Note 20)		36	80	
		Ind/Mil (Note 21)		58	95	
I_{CC4}	Active Current (TTL) (SRAM Block Selected) (Notes 17 and 19)	Comm'l (Note 20)		67	105	mA
		Comm'l (Note 21)		79	120	
		Ind/Mil (Note 20)		67	130	
		Ind/Mil (Note 21)		79	145	
I_{LI}	Input Leakage Current	V_{IN} = 5.5 V or GND	−1	± 0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or GND	−10	± 5	10	

NOTE: 16. CMOS inputs: GND ± 0.3 V or V_{CC} ± 0.3V.
17. TTL inputs: $V_{IL} \leq 0.8$ V, $V_{IH} \geq 2.0$ V.
18. $\overline{CSI}$/A19 is high and the part is in a power-down configuration mode.
19. AC power component is 3.0 mA/MHz (power = AC + DC).
20. Ten (10) PAD product terms active. (Add 380 µA per product term, typical, or 480 µA per product term maximum
21. Forty-one (41) PAD product terms active.

AC Characteristics (See Timing Diagrams)

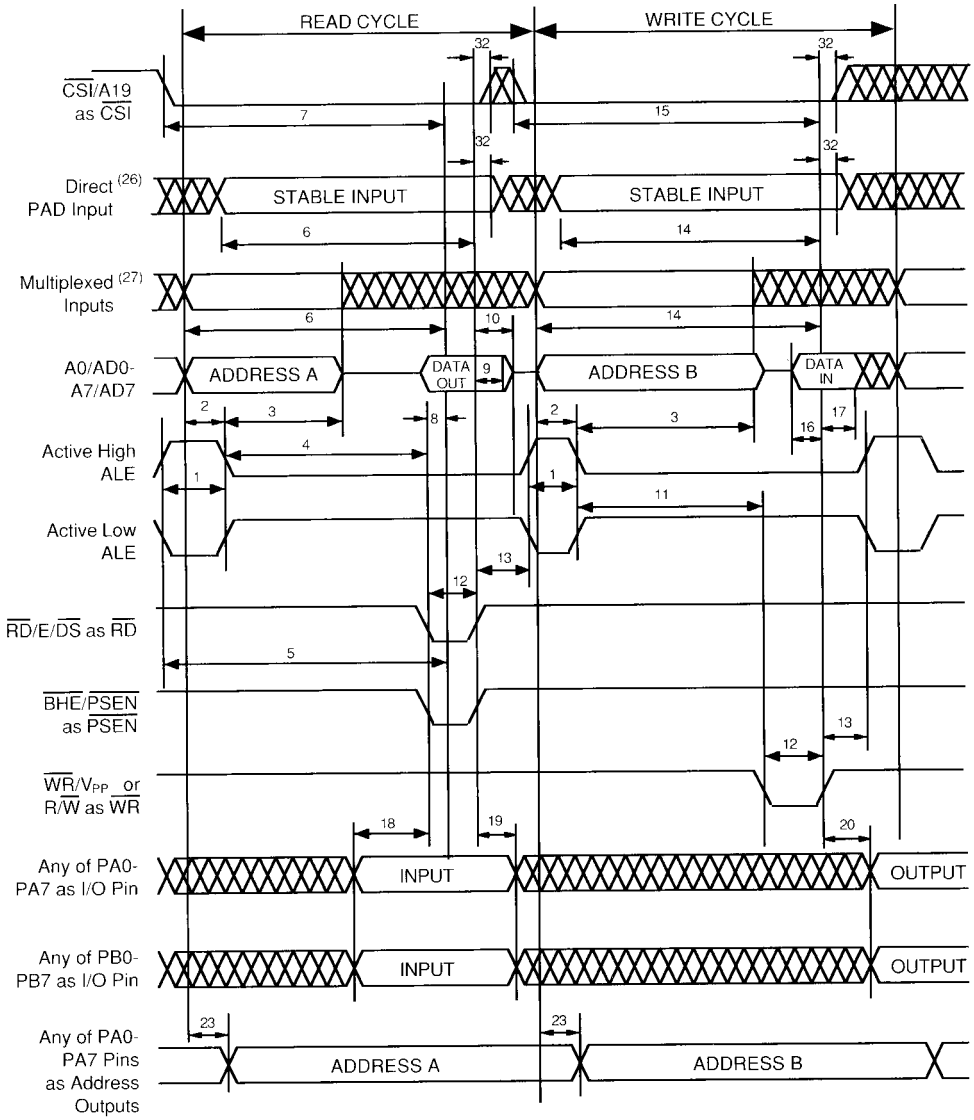
Symbol	Parameter	-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	
T1	ALE or AS Pulse Width	30		40		50		ns
T2	Address Set-up Time	9		12		15		
T3	Address Hold Time	9		12		15		
T4	ALE or AS Trailing Edge to Leading Edge of Read	12		15		20		
T5	ALE Valid to Data Valid	130		140		170		
T6	Address Valid to Data Valid		120		150		200	
T7	$\overline{CSI}$ Active to Data Valid		130		160		200	
T8	Leading Edge of Read to Data Valid		38		55		60	
T9	Read Data Hold Time	0		0		0		
T10	Trailing Edge of Read to Data High-Z		32		35		40	
T11	Trailing Edge of ALE or AS to Leading Edge of Write	12		15		20		
T12	$\overline{RD}$, E, $\overline{PSEN}$, $\overline{DS}$ pulse width	45		60		75		
T12A	$\overline{WR}$ Pulse Width	25		35		45		
T13	Trailing Edge of Write or Read to Leading Edge of ALE or AS	0		0		0		
T14	Address Valid to Trailing Edge of Write	120		150		200		

AC Characteristics (Cont.)

Symbol	Parameter	-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	
T15	$\overline{CSI}$ Active to Trailing Edge of Write	130		160		200		ns
T16	Write Data Set-up Time	20		30		40		
T17	Write Data Hold Time	5		10		15		
T18	Port Input Set-up Time	30		35		45		
T19	Port Input Hold Time	0		0		0		
T20	Trailing Edge of Write to Port Output Valid	40		50		60		
T21	ADi or Control to $\overline{CSOi}$ Valid	6	35	6	40	5	45	
T22	ADi or Control to $\overline{CSOi}$ Invalid	5	35	4	40	4	45	
T23	Track Mode Address Propagation Delay: CSADOUT1 Already True		22		28		28	
T23A	Track Mode Address Propagation Delay: CSADOUT1 Becomes True During ALE or AS		33		50		50	
T24	Track Mode Address Holding Time	15		27		27		
T25	Track Mode Read Propagation Delay		29		35		35	
T26	Track Mode Read Hold Time	11	29	10	29	10	35	
T27	Track Mode Write Cycle Data Propagation Delay		20		30		30	
T28	Track Mode Write Cycle Write to Data Propagation Delay	8	30	7	40	7	55	
T29	Hold Time of Port A Valid During Write $\overline{CSOi}$ Trailing Edge	2		4		4		
T30	$\overline{CSI}$ Active to $\overline{CSOi}$ Active	9	45	9	55	8	60	
T31	$\overline{CSI}$ Inactive to $\overline{CSOi}$ Inactive	9	45	9	55	8	60	
T32	Direct PAD Input as Hold Time	10		12		15		
T33	R/$\overline{W}$ Active to E or $\overline{DS}$ Start	20		30		40		
T34	E or $\overline{DS}$ End to R/$\overline{W}$	20		30		40		
T35	AS Inactive to E high	15		20		25		

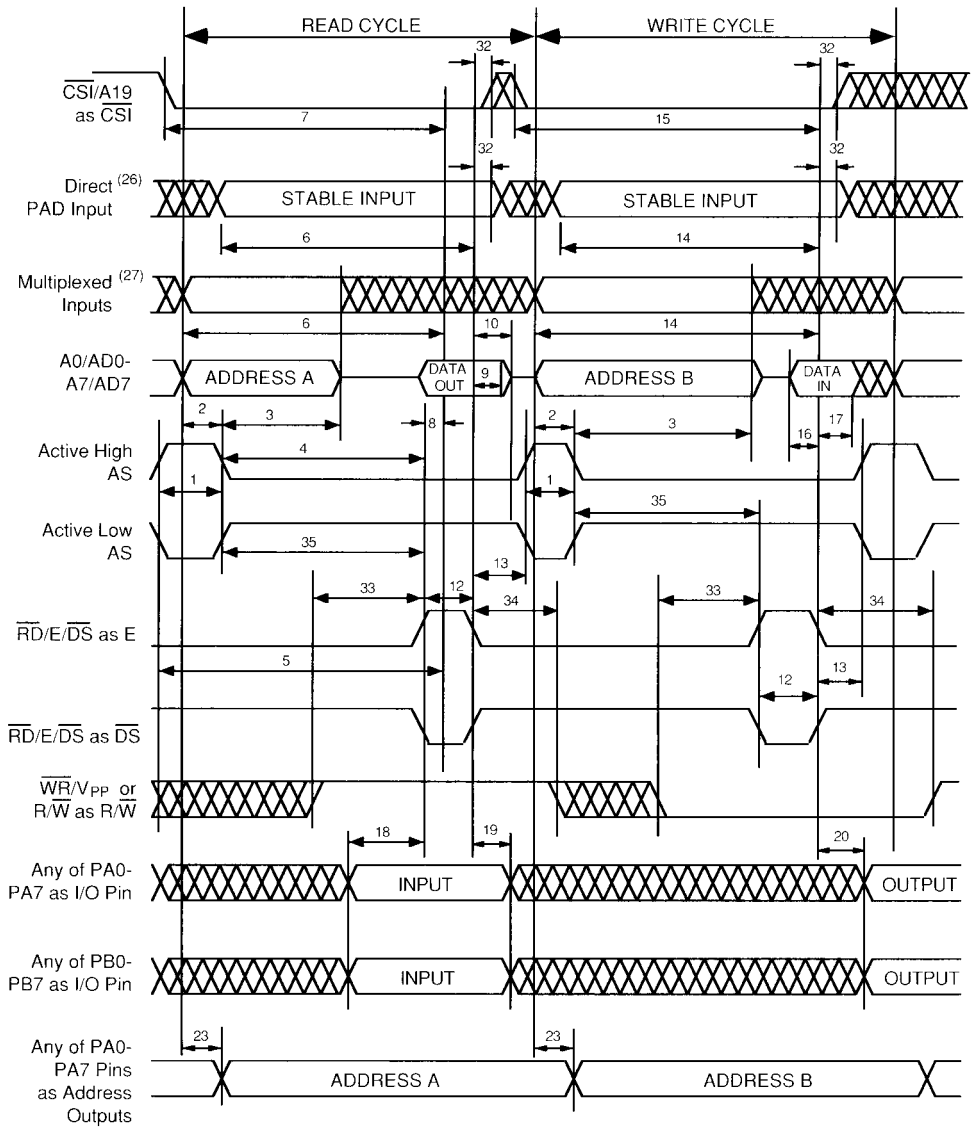
NOTES: 22. ADi = any address line.
23. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
24. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE (or AS).
25. Control signals $\overline{RD}$/E/$\overline{DS}$ or $\overline{WR}$ or R/$\overline{W}$.

Figure 15. Timing of 8-Bit Multiplexed Address/Data Bus, CRRWR = 0



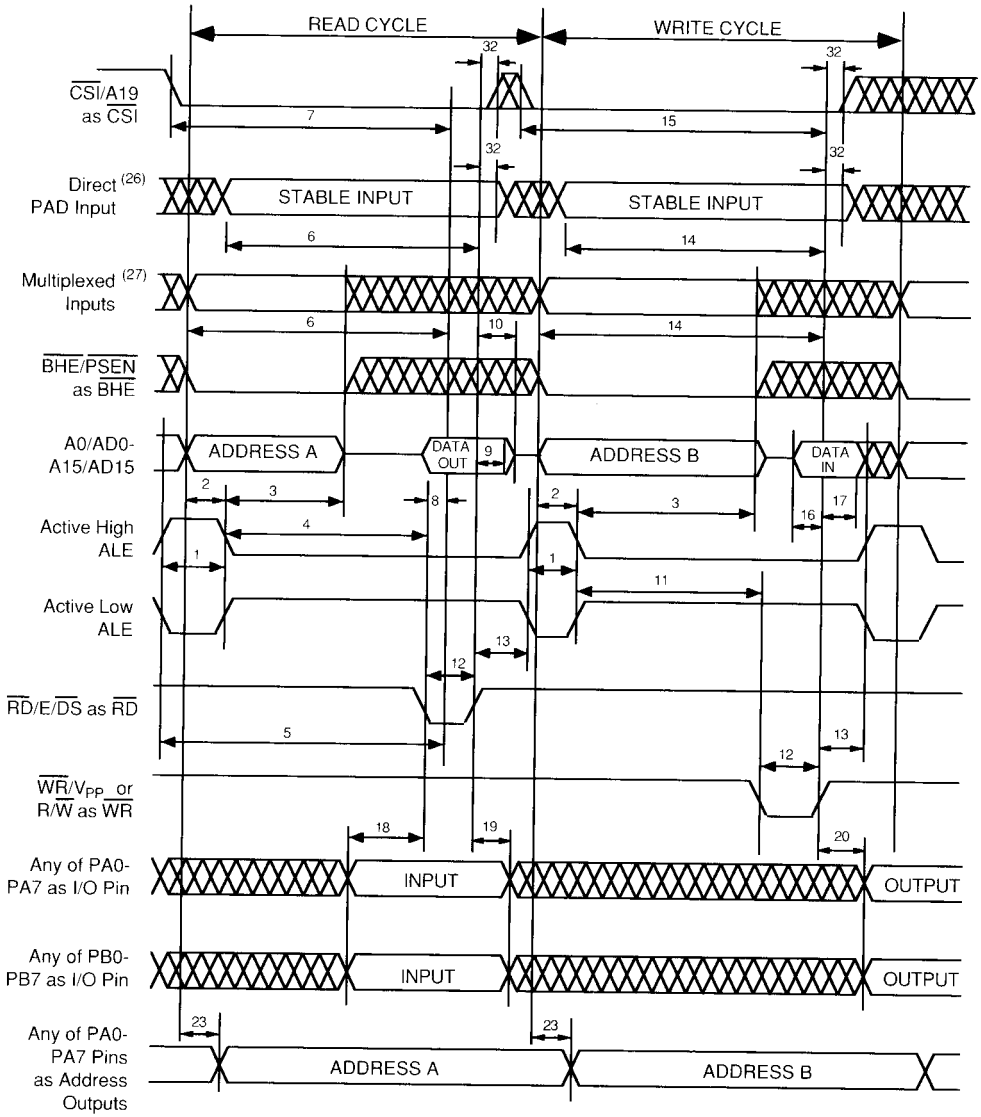
See referenced notes on page 2-119.

Figure 16. Timing of 8-Bit Multiplexed Address/Data Bus, CRRWR = 1



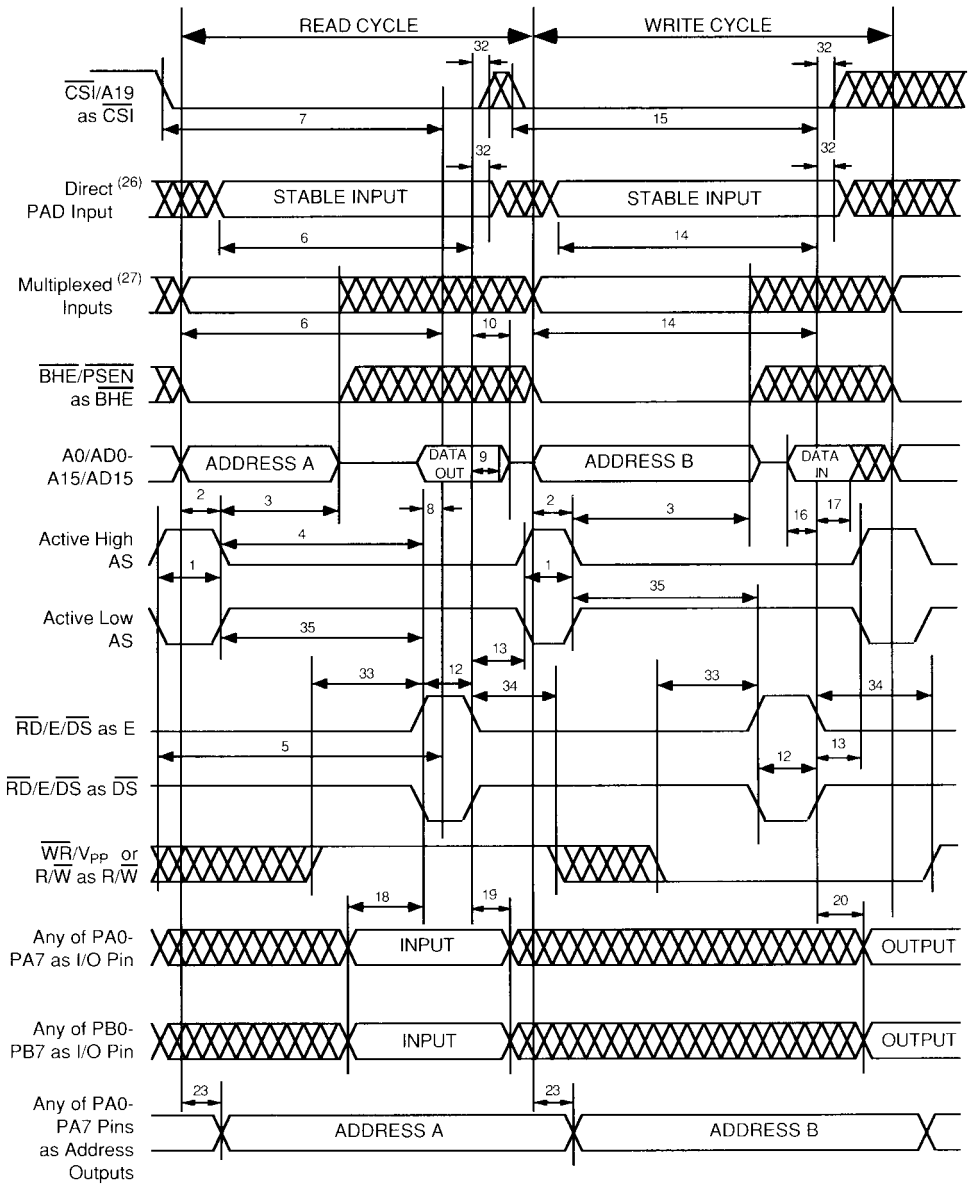
See referenced notes on page 2-119.

Figure 17. Timing of 16-Bit Multiplexed Address/Data Bus, CRRWR = 0



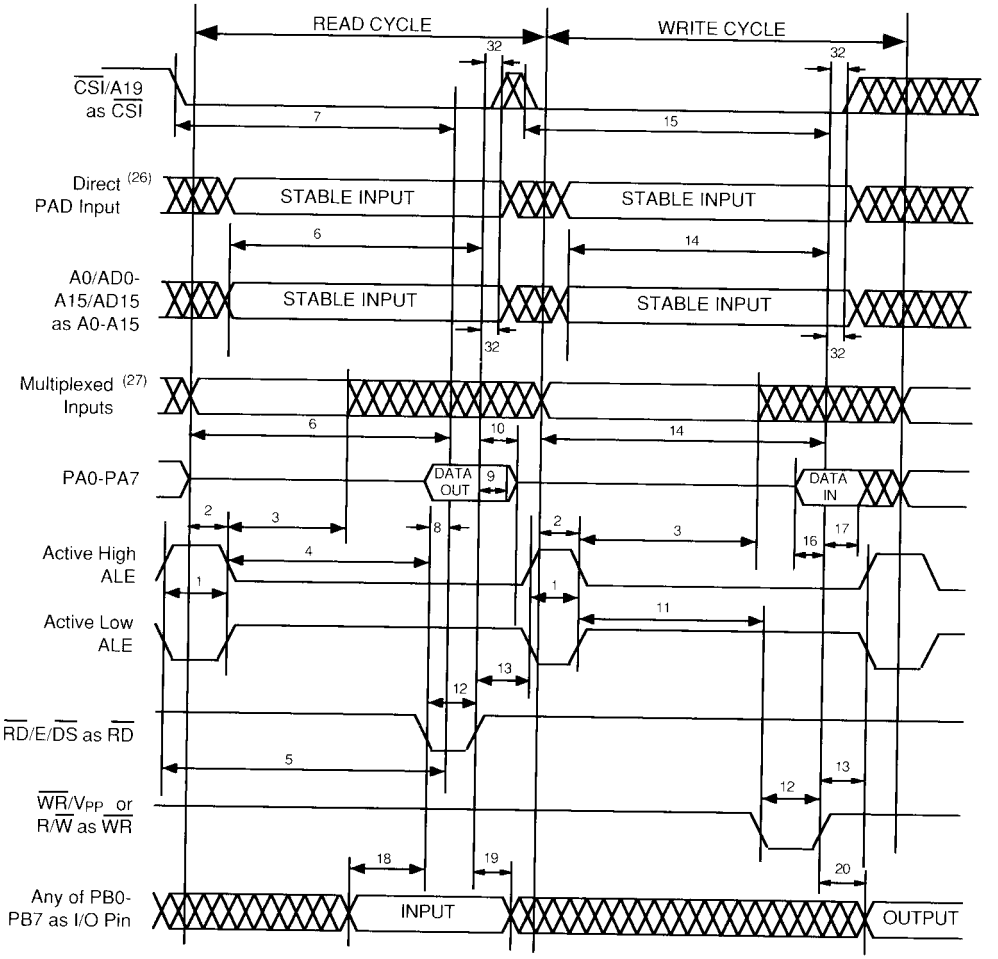
See referenced notes on page 2-119.

Figure 18. Timing of 16-Bit Multiplexed Address/Data Bus, CRRWR = 1



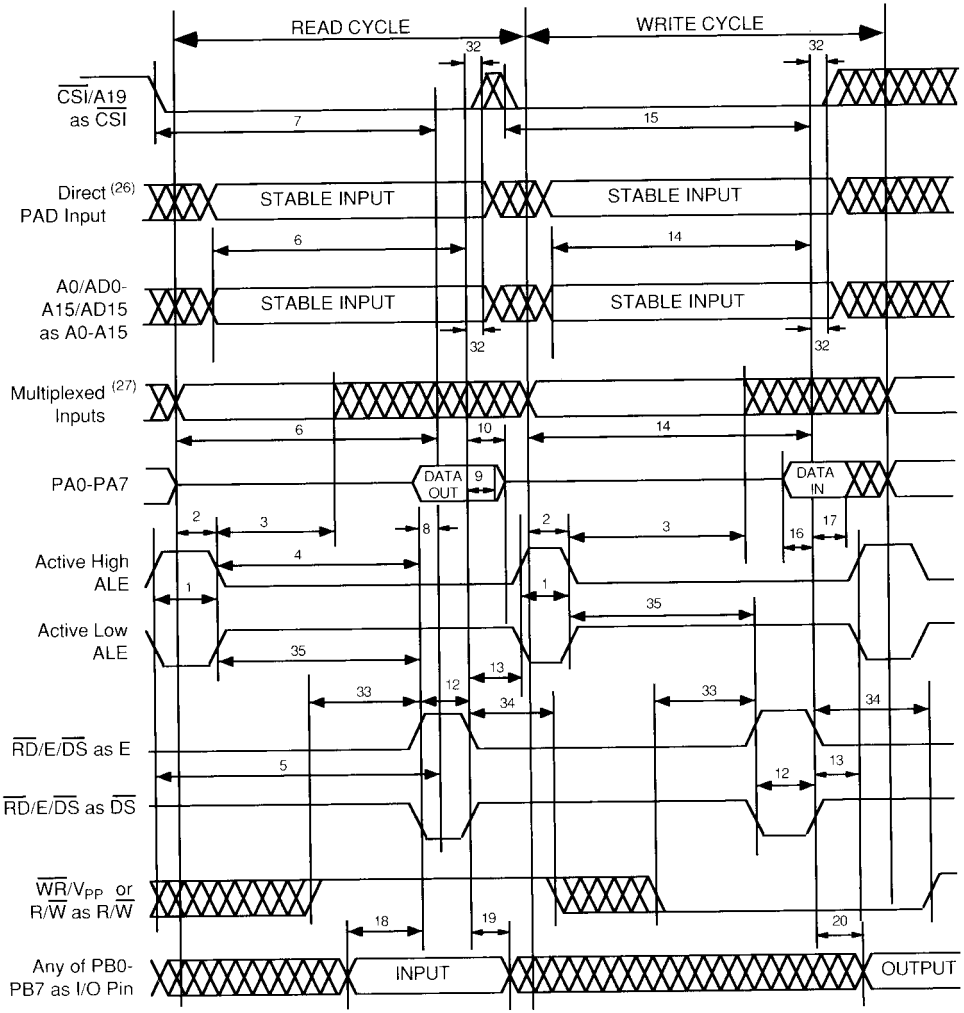
See referenced notes on page 2-119.

Figure 19. Timing of 8-Bit Data Non-Multiplexed Address/Data Bus, CRRWR = 0



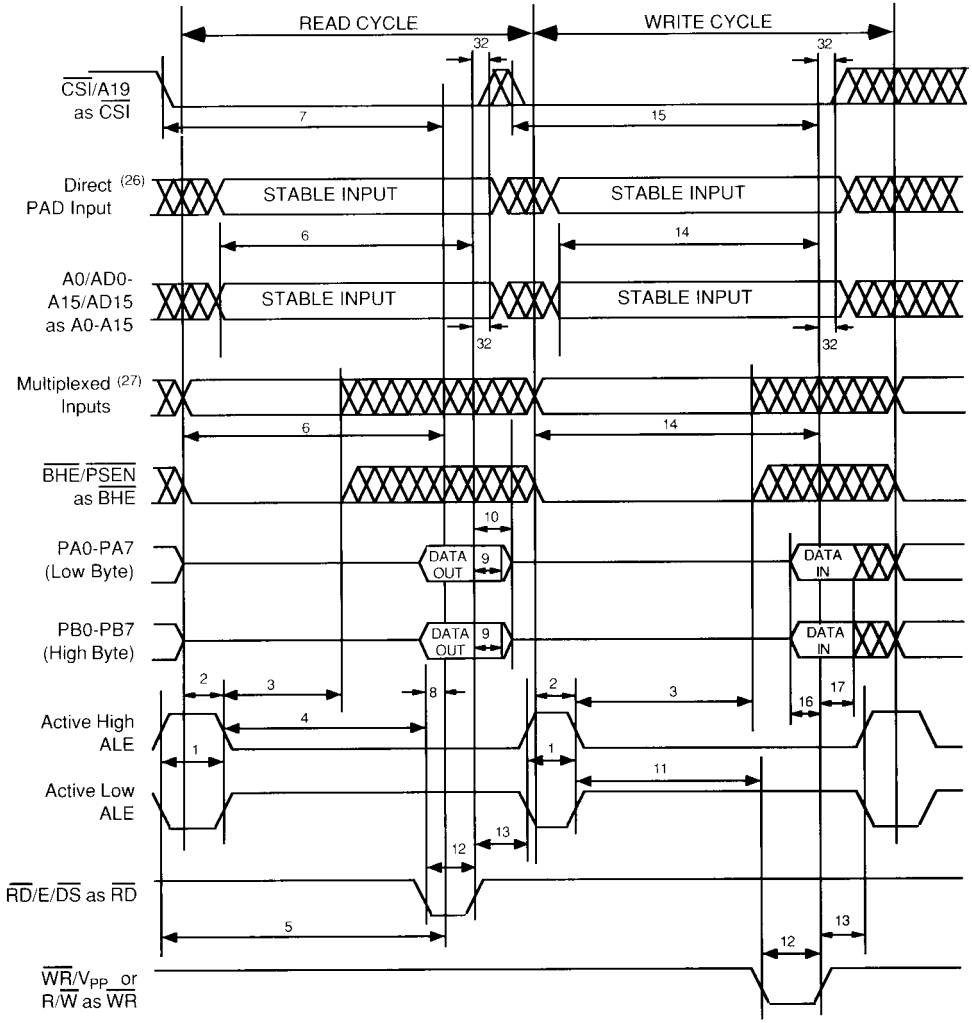
See referenced notes on page 2-119.

Figure 20. Timing of 8-Bit Data Non-Multiplexed Address/Data Bus, CRRWR = 1



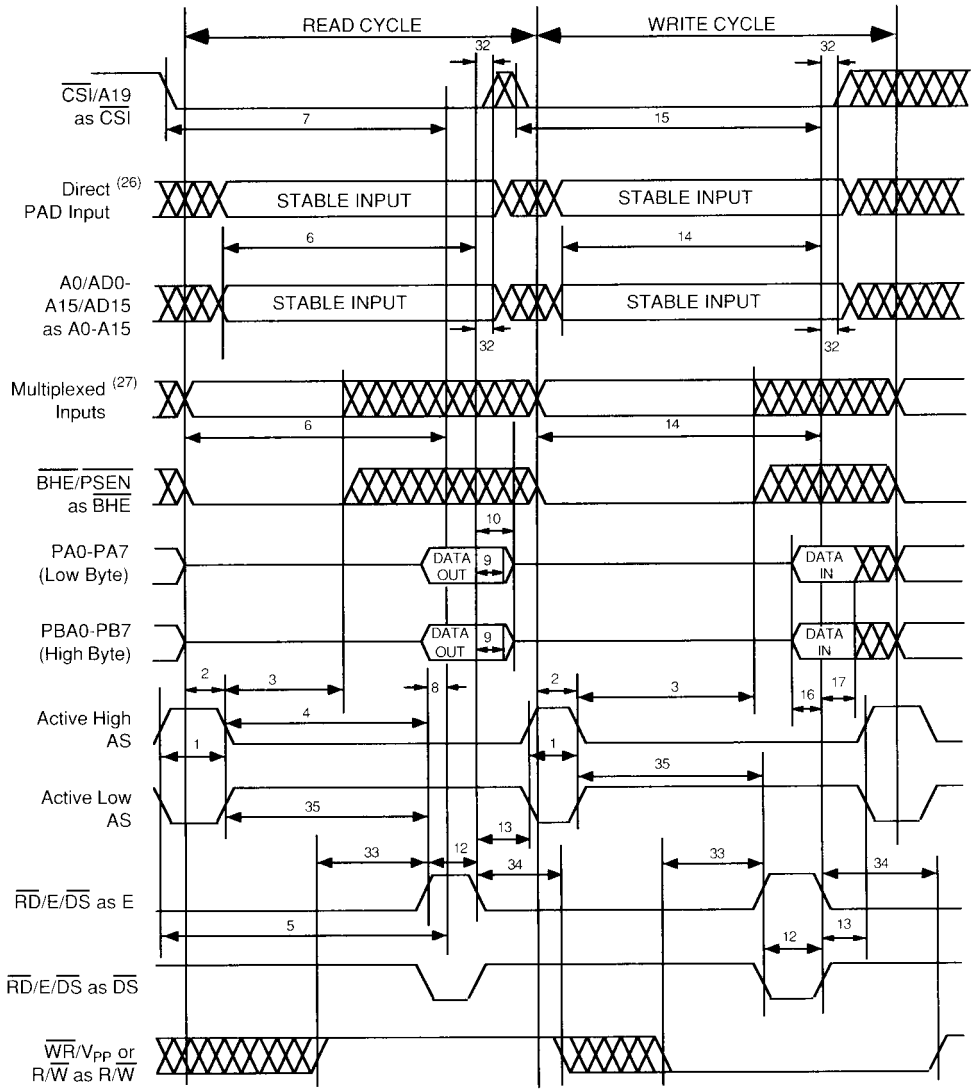
See referenced notes on page 2-119.

Figure 21. Timing of 16-Bit Non-Multiplexed Address/Data Bus, CRRWR = 0



See referenced notes on page 2-119.

Figure 22. Timing of 16-Bit Non-Multiplexed Address/Data Bus, CRRWR = 1



See referenced notes on page 2-119.

Figure 23. Chip-Select Output Timing

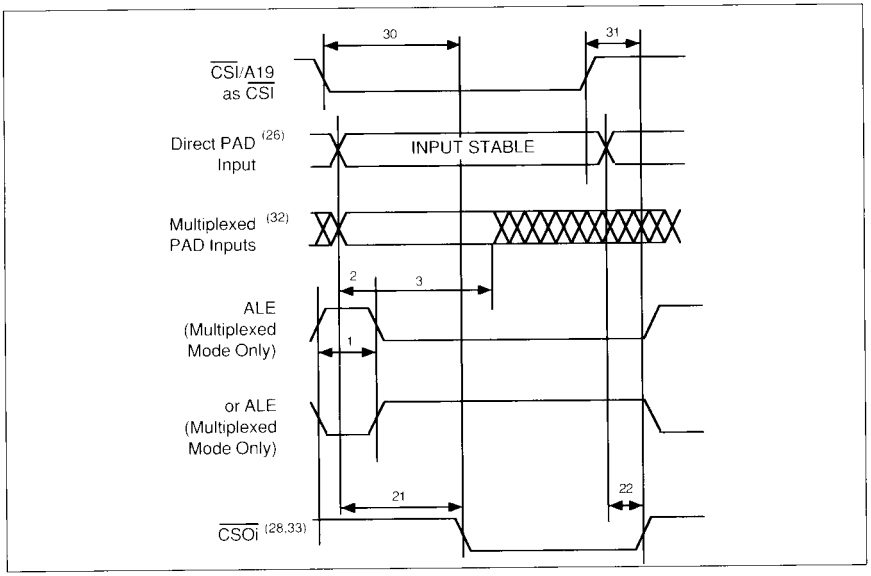
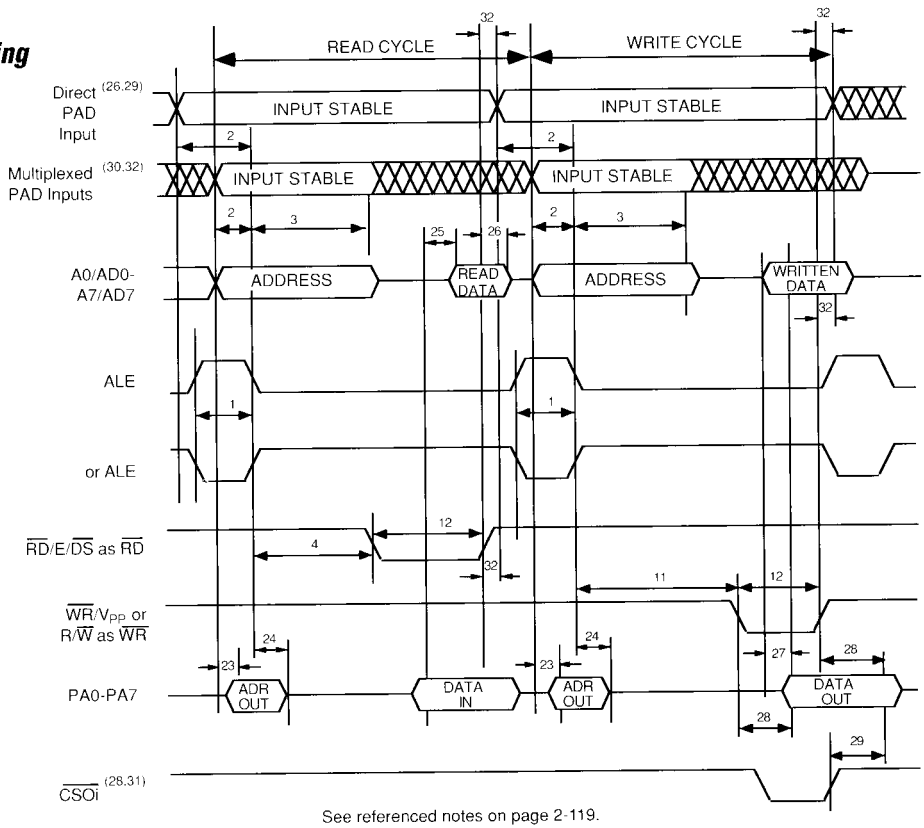
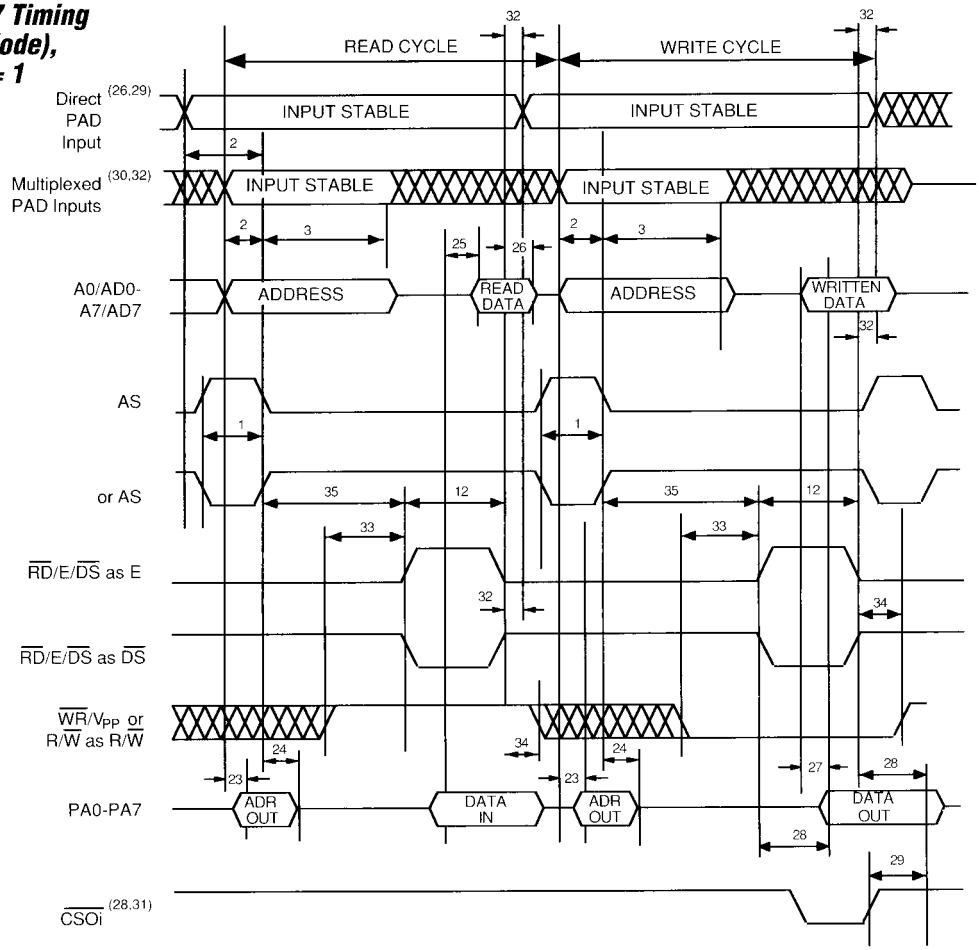


Figure 24. Port A as AD0–AD7 Timing (Track Mode), CRRWR = 0



See referenced notes on page 2-119.

Figure 25. Port A as AD0–AD7 Timing (Track Mode), CRRWR = 1



Notes for Timing Diagrams

26. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE in non-multiplexed modes.
27. Multiplexed inputs: any of the following inputs that are latched by the ALE (or AS): A0/AD0–A15/AD15, $\overline{CSI}$/A19 as ALE dependent A19, ALE dependent PC0–PC2.
28. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
29. CSADOUT1, which internally enables the address transfer to Port A, should be derived only from direct PAD input signals, otherwise the address propagation delay is slowed down.
30. CSADIN and CSADOUT2, which internally enable the data-in or data-out transfers, respectively, can be derived from any combination of direct PAD inputs and multiplexed PAD inputs.
31. The write operation signals are included in the $\overline{CSOi}$ expression.
32. Multiplexed PAD inputs: any of the following PAD inputs that are latched by the ALE (or AS) in the multiplexed modes: A11/AD11–A15/AD15, $\overline{CSI}$/A19 as ALE dependent A19, ALE dependent PC0–PC2.
33. $\overline{CSOi}$ product terms can include any of the PAD input signals shown in Figure 3, except for reset and $\overline{CSI}$.

Table 14. Pin Capacitance[34]

T_A = 25 °C, f = 1 MHz

Symbol	Parameter	Conditions	Typical[35]	Max	Unit
C_{IN}	Capacitance (for input pins only)	V_{IN} = 0 V	4	6	pF
C_{OUT}	Capacitance (for input/output pins)	V_{OUT} = 0 V	8	12	pF
C_{VPP}	Capacitance (for $\overline{WR}/V_{PP}$ or $R/\overline{W}/V_{PP}$)	V_{PP} = 0 V	18	25	pF

NOTES: 34. This parameter is only sampled and is not 100% tested.
35. Typical values are for T_A = 25°C and nominal supply voltages.

Figure 26. AC Testing Input/Output Waveform

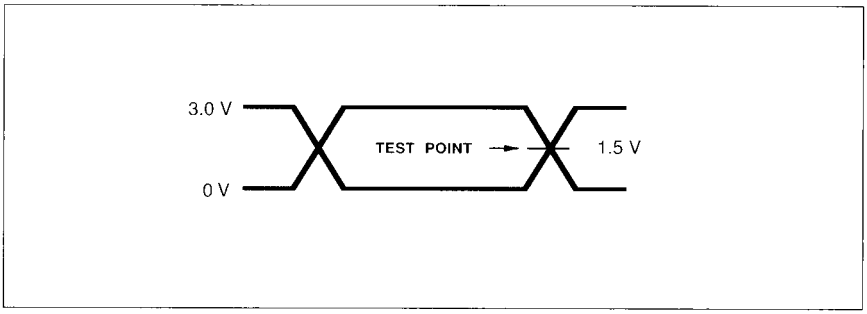
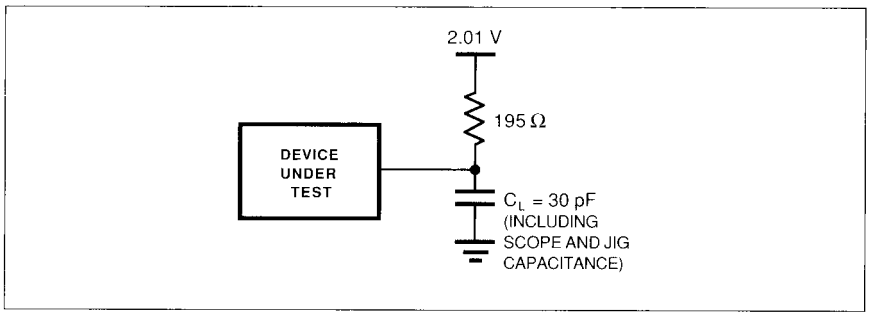


Figure 27. AC Testing Load Circuit



Erasure and Programming

To clear all locations of their programmed contents, expose the device to ultra-violet light source. A dosage of 15 W second/cm² is required. This dosage can be obtained with exposure to a wavelength of 2537 Å and intensity of 12000 µW/cm² for 15 to 20 minutes. The device should be about 1 inch from the source, and all filters should be removed from the UV light source prior to erasure.

The PSD302 and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although the erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight eventually erases the device. For maximum system reliability, these sources should be avoided. If used in such an environment, the package windows should be covered by an opaque substance.

Upon delivery from WSI, or after each erasure, the PSD302 device has all bits in the PAD and EPROM in the "1" or high state. The configuration bits are in the "0" or low state. The code, configuration, and PAD MAP data are loaded through the procedure of programming

Information for programming the device is available directly from WSI. Please contact your local sales representative.

Pin Assignments

Name	44-Pin PLDCC/ CLDCC Package	44-Pin CPGA Package	52-Pin PQFP Package
$\overline{BHE}/\overline{PSEN}$	1	A_5	46
$\overline{WR}/V_{PP}$ or $R/\overline{W}$	2	A_4	47
RESET	3	B_4	48
PB7	4	A_3	49
PB6	5	B_3	50
PB5	6	A_2	51
PB4	7	B_2	2
PB3	8	B_1	3
PB2	9	C_2	4
PB1	10	C_1	5
PB0	11	D_2	6
GND	12	D_1	7
ALE or AS	13	E_1	8
PA7	14	E_2	9
PA6	15	F_1	10
PA5	16	F_2	11
PA4	17	G_1	12
PA3	18	G_2	15
PA2	19	H_2	16
PA1	20	G_3	17
PA0	21	H_3	18
$\overline{RD}/E/\overline{DS}$	22	G_4	19
AD0/A0	23	H_4	20
AD1/A1	24	H_5	21
AD2/A2	25	G_5	22
AD3/A3	26	H_6	23
AD4/A4	27	G_6	24
AD5/A5	28	H_7	25
AD6/A6	29	G_7	28
AD7/A7	30	G_8	29
AD8/A8	31	F_7	30
AD9/A9	32	F_8	31
AD10/A10	33	E_7	32
GND	34	E_8	33
AD11/A11	35	D_8	34
AD12/A12	36	D_7	35
AD13/A13	37	C_8	36
AD14/A14	38	C_7	37
AD15/A15	39	B_8	38
PC0	40	B_7	41
PC1	41	A_7	42
PC2	42	B_6	43
A19/$\overline{CSI}$	43	A_6	44
V_{CC}	44	B_5	45

NOTE: 36. Pins 1, 13, 14, 26, 27, 39, 40, and 52 are No Connect.

Package Information

Figure 28. Drawing L4 — 44 Pin Ceramic Leaded Chip Carrier (CLDCC) with Window (Package Type L)

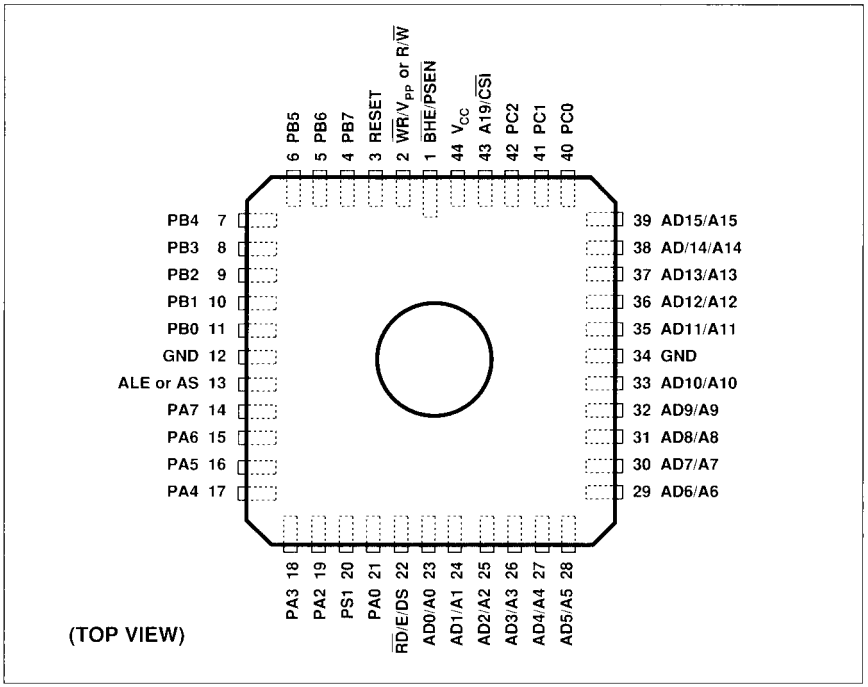


Figure 29. Drawing J2 — 44-Pin Plastic Leaded Chip Carrier (PLDCC) (Package Type J)

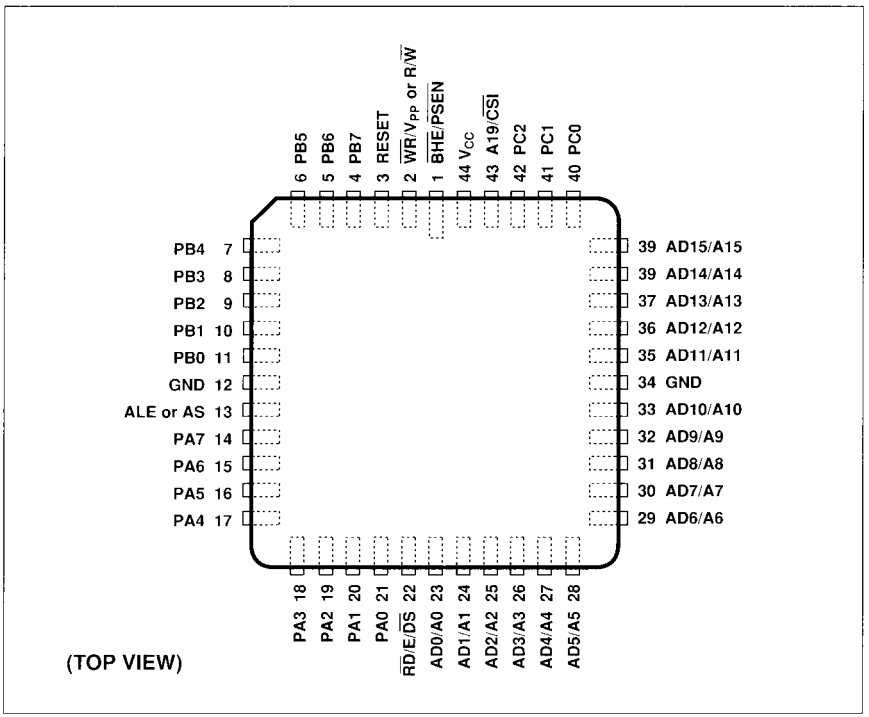


Figure 30. Drawing Q2 — 52-Pin PQFP (Package Type Q)

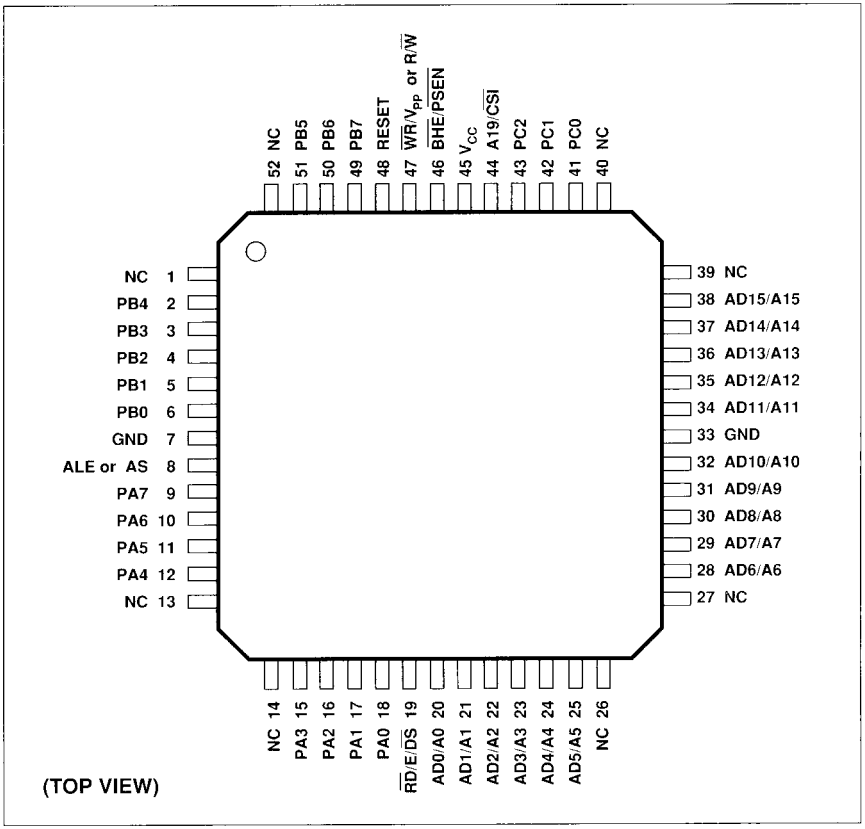
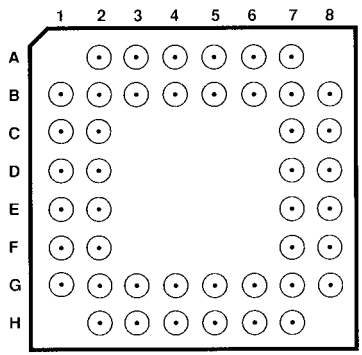


Figure 31: Drawing X2 — 44-Pin CPGA (Package Type X)



(TOP VIEW, THROUGH PACKAGE)

Ordering Information

Part Number	Spd. (ns)	Package Type	Package Drawing	Operating Temperature Range	WSI Manufacturing Procedure
PSD302-12J	120	44-pin PLDCC	J2	Commercial	Standard
PSD302-12L	120	44-pin CLDCC	L4	Commercial	Standard
PSD302-12Q	120	52-pin PQFP	Q2	Commercial	Standard
PSD302-12X	120	44-pin CPGA	X2	Commercial	Standard
PSD302-15J	150	44-pin PLDCC	J2	Commercial	Standard
PSD302-15JI	150	44-pin PLDCC	J2	Industrial	Standard
PSD302-15L	150	44-pin CLDCC	L4	Commercial	Standard
PSD302-15LI	150	44-pin CLDCC	L4	Industrial	Standard
PSD302-15LM	150	44-pin CLDCC	L4	Military	Standard
PSD302-15LMB	150	44-pin CLDCC	L4	Military	MIL-STD-883C
PSD302-15Q	150	52-pin PQFP	Q2	Commercial	Standard
PSD302-15X	150	44-pin CPGA	X2	Commercial	Standard
PSD302-15XI	150	44-pin CPGA	X2	Industrial	Standard
PSD302-15XM	150	44-pin CPGA	X2	Military	Standard
PSD302-15XMB	150	44-pin CPGA	X2	Military	MIL-STD-883C
PSD302-20J	200	44-pin PLDCC	J2	Commercial	Standard
PSD302-20JI	200	44-pin PLDCC	J2	Industrail	Standard
PSD302-20L	200	44-pin CLDCC	L4	Commercial	Standard
PSD302-20LI	200	44-pin CLDCC	L4	Industrial	Standard
PSD302-20LM	200	44-pin CLDCC	L4	Military	Standard
PSD302-20LMB	200	44-pin CLDCC	L4	Military	MIL-STD-883C
PSD302-20Q	200	52-pin PQFP	Q2	Commercial	Standard
PSD302-20X	200	44-pin CPGA	X2	Commercial	Standard
PSD302-20XI	200	44-pin CPGA	X2	Industrial	Standard
PSD302-20XM	200	44-pin CPGA	X2	Military	Standard
PSD302-20XMB	200	44-pin CPGA	X2	Military	MIL-STD-883C